Technical Manual

COMPONENTS GUIDE

015-000028-03

DATA GENERAL TECHNICAL MANUAL

COMPONENTS GUIDE

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The purpose of this manual is to provide part number identification of components used in Data General equipment. Pin connections, logic diagrams, truth tables and functional descriptions are included in the Integrated Circuits section. In the Circuit Modules section, pin connections and block diagrams are furnished.

It is not the purpose of this manual to provide manufacturers' specifications or circuit parameters.

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DGC Part Number	Functional Description
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DGC Part Number	Functional Description
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100000131	General Purpose Transistor Array
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100000133	Hex Inverter
100000134	4-Bit Data Selector/Storage Register

DGC Part Number	Functional Description
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100000136	8-Input Priority Encoder
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100000141	256-Bit Bipolar Read Only Memory
100000142	256-Bit Bipolar Read Only Memory
100000143	BCD-To-Decimal Decoder/Driver
100000144	5-Bit Comparator
100000145	8-Bit Addressable Latch
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100000162	Dual J-K Master/Slave Flip-Flop with Separate Clears and Clocks
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100000171	16-Bit Multiple-Port Register File with 3-State Outputs
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100000173	Dual 4-Input Positive-NAND 50 Ohm Line Driver

DGC Part Number	Functional Description
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100000182	4-2-3-2-Input AND-OR-INVERT Gates
100000185	Decoder/Demultiplexer
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100000187	Quadruple 2-Line-To-1-Line Data Selector/Multiplexer
100000188	Hex Inverter with Open-Collector Outputs
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100000194	Quad MOS Clock Driver
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100000198	Synchronous 4-Bit Counter
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100000201	Quadruple 2-Input Multiplexer with Storage
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100000204	Hex D-Type Flip-Flops with Clear
100000205	Quadruple D-Type Flip-Flops with Clear
100000206	4-Bit Quad Exclusive-NOR Gates
100000207	9-Bit Parity Generator and Checker
100000208	256-Bit Bipolar Programmable ROM (32x8 PROM)
100000211	16-Bit Associative-Content Addressable Memory
100000214	2048-Bit MOS LSI Random Access Memory
100000215	256-Bit Bipolar Read Only Memory
100000216	256-Bit Bipolar Read Only Memory
100000217	256-Bit Bipolar Read Only Memory
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DGC Part Number	Functional Description
100000219	256-Bit Bipolar Read Only Memory
100000221	Expandable Dual 2-Wide 2-Input AND-OR Invert Gate
100000222	Dual Retriggerable Monostable Multivibrator with Clear
100000223	Decoder/Demultiplexer
100000224	16-Channel Analog Multiplexer Complementary MOS (CMOS)
100000225	8-Channel Differential Analog Multiplexer Complementary MOS (CMOS)
100000226	High Speed Fully Decoded 64-Bit Memory
100000227	Presettable High Speed Binary Counter
100000228	Dual Peripheral Driver
100000229	Dual Sense Amplifier
100000231	Dual Peripheral Driver
100000232	1024-Bit Field Programmable Bipolar PROM
100000233	Quadruple 2-Line-To-1-Line Data Selector/Multiplexer
100000234	4-Bit Bidirectional Universal Shift Register
100000235	Triple 3-Input Positive-NAND Gate
100000236	2-Input, 4-Bit Digital Multiplexer
100000237	Triple 3-Input Positive-AND Gate
100000238	Dual Peripheral Driver
100000240	Quadruple 2-Line-To-1-Line Data Selector/Multiplexer
100000241	256-Bit Read-Write Memory with 3-State Outputs
100000242	Four-Channel Programmable Amplifier
100000243	Wide Band, High Impedance Operational Amplifier
100000244	High Slew Rate F. E. T. Input Operational Amplifier
100000245	1024-Bit Bipolar Programmable ROM (256x4 PROM, Open Collector)
100000247	Dual Peripheral Driver
100000248	Sense Amplifier
100000249	Positive-NAND Gate
100000250	Quad Exclusive OR Gate
100000252	Up/Down BCD Decade Counter
100000255	256-Bit Bipolar Random Access Memory
100000256	1024-Bit Programmable Bipolar Read Only Memory
100000257	Dual D-Type Edge-Triggered Flip-Flop
100000258	256-Bit Bipolar (32x8) Electrically Programmable Read Only Memory
100000259	Triple 3-Input Positive-AND Gate with Open-Collector Outputs
100000260	Triple 3-Input Positive-NOR Gate

DGC Part Number	Functional Description
100000261	Phase Locked Loop
100000262	Quadruple 2-Input Positive-NOR Gate
100000263	BCD-To-Seven-Segment Decoder/Driver
100000264	Dual 4-Input Positive-NAND Buffer
100000265	Hex Schmitt-Trigger Inverter
100000266	64-Bit Random Access Read/Write Memory
100000267	Operational Amplifier
100000268	Dual Operational Amplifier
100000269	256-Bit Bipolar Read Only Memory
100000270	256-Bit Bipolar Read Only Memory
100000271	256-Bit Bipolar Read Only Memory
100000272	256-Bit Bipolar Read Only Memory
100000273	256-Bit Bipolar Read Only Memory
100000274	256-Bit Bipolar Read Only Memory
100000275	256-Bit Bipolar Read Only Memory
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100000278	256-Bit Bipolar Read Only Memory
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100000280	256-Bit Bipolar Read Only Memory
100000281	Quadruple 2-Input Positive-NAND Schmitt Trigger
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100000283	Low Power Dual Retriggerable Resettable Monostable Multivibrator
100000284	Hex Inverter with Open-Collector Outputs
100000287	9-Bit Odd/Even Parity Generator/Checker
100000290	Three-Terminal Negative Regulator
100000292	Voltage Comparator/Buffer
100000293	Operational Amplifier
100000294	Operational Amplifier
100000295	Dual Line Receiver
100000296	4-Bit Magnitude Comparator
100000297	Data Selector/Multiplexer
100000298	Dual Sense Amplifier
100000299	Dual Sense Amplifier

DGC Part Number	Functional Description
100000300	Dual D-Type Edge-Triggered Flip-Flop
100000301	Phase-Frequency Detector
100000304	Dual Line Driver
100000305	Dual 5-Input Positive-NOR Gate
100000306	Arithmetic Logic Unit/Function Generator
100000307	Memory Driver w/Decode Inputs
100000309	NAND Gate
100000310	Quadruple 2-Input NAND Gate
100000311	Quadruple 2-Input NAND Power Gate
100000312	10-Input NAND Gate
100000313	Dual J-K Flip-Flop w/Individual Clocks and Presets
100000314	Differential Video Amplifier
100000316	Dual F-K Flip-Flop w/Common Clocks and Clears
100000317	Triple 3-Input NAND Gate
100000318	Precision Voltage Regulator
100000319	High Performance Operational Amplifier
100000320	Operational Amplifier
100000321	Dual Retriggerable Resettable Monostable Multivibrator
100000322	Dual Differential Comparator
100000323	Dual 4-Input NAND Power Gate w/Expander
100000324	High Speed Differential Comparator
100000325	Dual Differential Amplifier
100000326	Differential Video Amplifier
100000327	Triple 3-Input Positive NAND Gate
100000330	Quadruple 2-Input Positive-NOR Gate
100000331	4-Bit Binary and Decade Counters
100000332	Channel Junction F. E. T.
100000333	Operational Amplifier
100000334	Triple 3-Input NAND Gate
100000337	8-Input Positive NAND Gate
100000338	Dual 4-Input Positive NAND Gate
100000339	Triple 3-Input Positive NAND Gate
100000340	Quadruple 2-Input Positive NAND Gate
100000341	Quadruple 2-Input Positive NOR Gate
100000342	Dual J-K Flip-Flop w/Preset and Clear
100000343	Dual Comparator
100000344	Operational Amplifier
100000347	256-Bit Bipolar (32x8) Electronically Programmable Read Only Memory

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DGC Part Number	Functional Description
100000430	1024-Bit Programmable Bipolar Read Only Memory
100000431	
100000432	
100000433	
100000434	
100000435	
100000436	Dual 144-Bit Mask-Programmable Shift Register
100000437	1024-Bit Programmable Bipolar Read Only Memory
100000438	256-Bit Bipolar (32x8) Electrically Programmable Read Only Memory
100000465	1024 x 1 Bit Bipolar RAM, Open-Collector
100000470	Voltage Comparator
100000472	Quadruple 2-Input Positive-NAND Gate
100000484	Three-Terminal Negative Regulator
100000485	256-Bit Bipolar (32x8) Electrically Programmable Read Only Memory
100000486	256-Bit Bipolar (32x8) Electrically Programmable Read Only Memory
100000487	MOS Clock Driver
100000491	1024-Bit Programmable Bipolar Read Only Memory
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100000496	
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100000499	256-Bit Bipolar Read Only Memory
100000500	
100000502	Dual Monostable Multivibrators w/Schmitt-Trigger inputs
100000504	Dual 2-Wide 2-Input AND-OR Invert Gate
100000505	Clock Driver
100000506	Sense Amplifier
100000508	Up/Down Decade Counter
100000509	BCD-To-Decimal Decoder
100000510	8-Bit Parallel-In Serial-Out Shift Register
100000511	8-Bit Serial-In Parallel-Out Shift Register
100000512	Up/Down Binary Counter
100000536	Asynchronous Receiver/Transmitter
100000540	High-Speed 6-Bit Identity Comparator
100000541	8-Bit Parallel-Out Shift Register
100000542	Parallel-Load 8-Bit Shift Register
100000545	Quad Line Receiver
100000546	Quad MDTL Line Driver
100000581	Synchronous 4-Bit Counters
100000590	4096-Bit Random Access Memory
100000625	Dual Peripheral Driver
100000626	Dual Peripheral Driver
100000627	Dual Peripheral Driver
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DGC Part Number	Function
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100000296	4-Bit Magnitude Comparator
100000144	5-Bit Comparator
100000068) 100000365)	Quadruple 2-Input Exclusive-OR Gate
100000250	Quad Exclusive-OR Gate
100000206	4-Bit Quad Exclusive-NOR Gate
100000067	8-Bit Odd/Even Parity Generator/Checker
100000207	9-Bit Parity Generator and Checker
100000287	9-Bit Odd/Even Parity Generator/Checker
100000100) 100000170)	Look Ahead Carry Generators
100000043	Arithmetic Logic Element
100000084) 100000169) 100000306)	Arithmetic Logic Units/Function Generators

CHARACTER GENERATOR

DGC Part Number	Function
100000150	High-Speed 64x7x5 Character Generator

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COMMUNICATIONS CIRCUITS

DGC Part Number	Function
100000024	Dual Differential Amplifier
100000132	Dual Stereo Preamplifier
100000062) 100000314) 100000326) 100000372)	Differential Video Amplifier
100000325	Dual Differential Amplifier

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COMPARATORS AND SENSE AMPLIFIERS

DGC Part Number	Function
100000060) 100000343)	Dual Comparator
100000059) 100000157)	High-Speed Differential Comparator
100000292	Voltage Comparator/Buffer
100000248	Sense Amplifier
100000052	Dual Sense Amplifier
100000118) 100000229) 100000298) 100000299)	Dual Sense Amplifiers
100000322	Dual Differential Comparator
100000470	Voltage Comparator
100000506	Sense Amplifier
100000540	High-Speed 6-Bit Identity Comparator

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COUNTERS

DGC Part Number	Function
100000161	Divide-By-Twelve Counter (Divide-By-Two and Divide-By-Six)
100000080) 100000227)	Presettable High-Speed Binary Counter
100000153	BCD Decade Counter
100000047	4-Bit Binary Counter
100000038	BCD Decade Counter/Storage Element
100000028	4-Bit Binary Counter/Storage Element
100000198	Synchronous 4-Bit Counter
100000252) 100000384)	Up/Down BCD Decade Counter
100000128	Up/Down 4-Bit Binary Counter
100000358	35-MHz Presettable Decade and Binary Counters/Latches
100000377	Divide-By-Twelve Counter/Storage Element
100000331	4-Bit Binary Counter
100000391	Decade Counter
100000392	4-Bit Binary Counter
100000508	Up/Down Decade Counter
100000512	Up/Down Binary Counter
100000581	Synchronous 4-Bit Counters

DECODERS/DEMULTIPLEXORS

DGC Part Number	Function
100000092	Dual One-Of-Four Decoder
100000013	One-Of-Ten Decoder
100000189	One-Of-Ten Decoder With Open Collector Output
100000178	BCD-To-Decimal Decoder
100000185) 100000223)	Decoders/Demultiplexors
100000147	Dual 2-Line-To-4-Line Decoder/Demultiplexor
100000077	BCD-To-Decimal Decoder/Driver
100000143	BCD-To-Decimal Decoder/Driver
100000263	BCD-To-Seven-Segment Decoder/Driver
100000079) 100000307)	Memory Driver With Decode Inputs
100000375	BCD-To-Decimal Decoder
100000509	BCD-To-Decimal Decoder

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FLIP-FLOPS/LATCHES

DGC Part Number	Function
100000011	Dual J-K Flip-Flop
100000053	Dual J-K Flip-Flop
100000115	Dual J-K Flip-Flop
100000160	Dual J-K Edge-Triggered Flip-Flops
100000162	Dual J-K Master/Slave Flip-Flop With Separate Clears and Clocks
100000172	Dual J-K Negative-Edge-Triggered Flip-Flops With Preset and Clear
100000017) 100000257) 100000300)	Dual D-Type Edge-Triggered Flip-Flop
100000104	Dual D-Type Positive-Edge-Triggered Flip-Flops With Preset and Clear
100000082	Quad D-Type Flip-Flop
100000199	Hex D-Type Flip-Flop With Clear
100000200	Quadruple D-Type Flip-Flop With Clear
100000204	Hex D-Type Flip-Flop With Clear
100000205	Quadruple D-Type Flip-Flop With Clear
100000050) 100000387)	4-Bit Bistable Latches
100000145	8-Bit Addressable Latch
100000313	Dual J-K Flip-Flop, Individual Clocks and Presets
100000316	Dual J-K Flip-Flop, Common Clocks and Clears
100000342	Dual J-K Flip-Flop With Preset and Clear

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GATES/BUFFERS

DGC Part Number	Function
100000089	Quad 2-Input AND Gate
100000126	Triple 3-Input AND Gate
100000237	Triple 3-Input Positive-AND Gate
100000259	Triple 3-Input Positive-AND Gate With Open-Collector Outputs
100000119	Dual 4-Input Positive-AND Gate
100000023) 100000356) 100000357)	Dual Pulse Shaper-Delay AND Gate
100000158) 100000340) 100000515)	Quadruple 2-Input Positive-NAND Gate
100000036	Quad 2-Input NAND Gate
100000046	Quad 2-Input NAND Gate
100000003	Quad 2-Input NAND Gate
100000073	Triple 3-Input NAND Gate
100000004	Triple 3-Input NAND Gate
100000235) 100000327) 100000339)	Triple 3-Input Positive-NAND Gate
100000249) 100000374)	Positive-NAND Gate
100000005) 100000009) 100000040)	Dual 4-Input NAND Gate
100000007	8-Input NAND Gate
100000195) 100000337)	8-Input Positive-NAND Gate
100000203	13-Input Positive-NAND Gate
100000175	Quadruple 2-Input Positive-NAND Gate With Open-Collector Outputs
100000174	Positive-NAND Gate With Open-Collector Outputs
100000019	Quad 2-Input NAND Interface Gate
100000173	Dual 4-Input Positive-NAND 50 Ohm Line Driver
100000281	Quadruple 2-Input Positive-NAND Schmitt Trigger
100000066	Dual 4-Input Positive-NAND Schmitt Trigger
100000116	Quadruple 2-Input Positive-NAND Buffer
100000081	Quadruple 2-Input Positive-NAND Buffer
100000264	Dual 4-Input Positive-NAND Buffer
100000078	Quadruple 2-Input Positive-NAND Buffer With Open-Collector Outputs

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GATES/BUFFERS (CONTINUED)

DGC Part Number	Function
100000063	Quad 2-Input OR Gate
100000072	Quad 2-Input OR Gate
100000045	Quad 2-Input NOR Gate
100000061	Quad 2-Input NOR Gate
100000262) 100000330) 100000341) 100000366)	Quadruple 2-Input Positive-NOR Gate
100000070	Dual 4-Input NOR Gate
100000107	Quad NOR Gate
100000123	Triple 3-Input NOR Gate
100000260	Triple 3-Input Positive-NOR Gate
100000069	Single 7-Input NOR Gate
100000196	Quadruple 2-Input Positive-NOR Buffer With Open-Collector Outputs
100000181	Expandable 4-Wide AND-OR Gate
100000182	4-2-3-2-Input AND-OR-INVERT Gate
100000008	Single Extendable AND-OR-INVERT Gate
100000221	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate
100000006	Dual Extendable AND-OR-INVERT Gate
100000049	Expandable 4-Input AND-OR-INVERT Gate
100000039	Dual Extender AND-OR-INVERT Gate
100000020) 100000071)	Hex Inverter
100000076	Hex Inverter
100000090	6-Input Hex Inverter
100000159	Hex Inverter
100000098	Hex Inverter
100000121	CMOS Hex Inverter
100000133	Hex Inverter
100000188) 100000284)	Hex Inverter With Open-Collector Outputs
100000265	Hex Schmitt-Trigger Inverter
100000305	Dual-5 Input Positive NOR Gate
100000399	Quadruple 2-Input Exclusive OR Gates W/Open-Collector Outputs
100000309	Hex Inverter
100000394	TTL-MOS Hex Inverter

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GATES/BUFFERS (CONTINUED)

DGC Part Number	Function
100000310	Quad 2-Input NAND Gate
100000393	Quad 2-Input TTL-MOS Interface Gate
100000311	Quad 2-Input NAND Power Gate
100000376	Dual 2-Wide 2-Input AND-OR-INVERT Gates (One Gate Expandable)
100000312	10-Input NAND Gate
100000363	Hex Inverter W/Expandable (open base) or Translator Inputs
100000317	Triple 3-Input NAND Gate
100000364	Quadruple 2-Input Positive NAND Gate W/Open-Collector Outputs
100000323	Dual 4-Input NAND Power Gate With Expander
100000360	Hex Inverter
100000334	Triple 3-Input NAND Gate
100000342	Dual J-K Flip-Flops W/Preset and Clear
100000338	Dual 4-Input Positive NAND Buffers
100000472	Quad 2-Input Positive-NAND Gate
100000630	Quad 2-Input Positive-NAND Buffer W/Open-Collector Outputs

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INTERFACE ELEMENTS

DGC Part Number	Function
100000146	Dual Line Driver
100000117) 100000154) 100000238) 100000247) 100000228)	Dual Peripheral Drivers
100000231) 100000385)	Dual Peripheral Driver
100000194	Quad MOS Clock Driver
100000091	Hex Buffer/Driver With Open-Collector High Voltage Outputs
100000122	Dual Line Receiver
100000295	Dual Line Receiver
100000105	Quad Line Receivers
100000124	Quadruple Line Receiver
100000197	Monostable Multivibrator
100000015	Retriggerable Monostable Multivibrator
100000222	Dual Retriggerable Monostable Multivibrator With Clear
100000106) 100000321)	Dual Retriggerable Resettable Monostable Multivibrator
100000283	Low Power Dual Retriggerable Resettable Monostable Multivibrator
100000114	Dual Voltage Controlled Multivibrator
100000130) 100000536)	Asynchronous Receiver/Transmitter
100000304	Dual Line Driver
100000502	Dual Monostable Multivibrators W/Schmitt-Trigger Inputs
100000487	MOS Clock Driver
100000505	Clock Driver
100000545	Quad Line Receiver
100000546	Quad MDTL Line Driver
100000625	Dual Peripheral Driver
100000626	Dual Peripheral Driver
100000627	Dual Peripheral Driver

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MEMORIES

DGC Part Number	Function
100000266	64-Bit Random Access Read/Write Memory
100000074	64-Bit Random Access Memory
100000226	High-Speed Fully Decoded 64-Bit Memory
100000164	256-Bit Bipolar Random Access Memory
100000190	High-Speed Fully Decoded 256-Bit Random Access Memory
100000255	256-Bit Bipolar Random Access Memory
100000241	256-Bit Read-Write Memory With 3-State Outputs
100000016	16-Bit Coincident Select Read-Write Memory
100000102) 100000103)	256-Bit Read/Write Memory and Decoder/Driver
100000214	2048-Bit MOD LSI Random Access Memory
100000211	16-Bit Associative-Content Addressable Memory
100000140) 100000141) 100000142) 100000148) 100000149) 100000215) 100000216) 100000217) 100000218) 100000219) 100000269) 100000270) 100000271) 100000272) 100000273) 100000274) 100000275) 100000276) 100000277) 100000278) 100000279) 100000280)	256-Bit Bipolar Read Only Memory
100000095) 100000096)	256-Bit Bipolar Read Only Memory
100000191	High-Speed Fully Decoded 1024-Bit Read Only Memory
100000208	256-Bit Bipolar Programmable ROM (32x8 PROM)
100000258	256-Bit Bipolar (32x8) Electrically Programmable Read Only Memory
100000256	1024-Bit Programmable Bipolar Read Only Memory
100000232	1024-Bit Field Programmable Bipolar PROM
100000245	1024-Bit Bipolar Programmable ROM (256x4 PROM, Open-Collector)
100000192	High-Speed Electrically Programmable 1024-Bit Read Only Memory
100000001	PNP Quad Core Driver
100000041	NPN Quad Core Driver
100000465	1024 x 1 Bit Bipolar RAM, Open-Collector
100000590	4096-Bit Random Access Memory

DG-02041

MULTIPLEXORS

DGC Part Number	Function
100000167) 100000187)	Quadruple 2-Line-To-1 Line Data Selector/Multiplexor
100000233) 100000240)	Quadruple 2-Line-To-1 Line Data Selector/Multiplexor
100000166	Dual 4-Line-To-1-Line Data Selector/Multiplexor
100000165	Data Selector/Multiplexor With 3-State Outputs
100000186	8-Line-To-1-Line Data Selector/Multiplexor
100000297	Data Selector/Multiplexor
100000057) 100000108)	2-Input, 4-Bit Digital Multiplexor
100000083	2-Input, 4-Bit Digital Multiplexor
100000236	2-Input, 4-Bit Digital Multiplexor
100000282	2-Input, 4-Bit Digital Multiplexor
100000129) 100000044)	3-Input, 4-Bit Digital Multiplexor
100000086	Quad Two-Input Multiplexor
100000201	Quadruple 2-Input Multiplexor With Storage
100000048	Dual Four-Input Multiplexor
100000075	Eight-Input Multiplexor
100000168	Dual 4-Line-To-1-Line Multiplexor
100000225	8-Channel Differential Analog Multiplexor Complementary MOS (CMOS)
100000224	16-Channel Analog Multiplexor Complementary MOS (CMOS)

DG-02042

OPERATIONAL AMPLIFIERS

DGC Part Numbers	Function
100000293	Operational Amplifier
100000294	Operational Amplifier
100000267	Operational Amplifier
100000156	High Performance Operational Amplifier
100000268	Dual Operational Amplifier
100000093	Monolithic Dual Operational Amplifier
100000242	Four Channel Programmable Amplifier
100000243	Wide Band, High Impedance Operational Amplifier
100000244	High Slew Rate F. E. T. Input Operational Amplifier
100000378	Monolithic Operational Amplifier
100000320	Monolithic Dual Operational Amplifier
100000333) 100000344)	Operational Amplifier

DG-02043

PHASE LOCKED LOOP

DGC Part Number	Function
100000261	Phase Locked Loop
100000120	Phase Locked Loop

DG-02044

REGISTERS

DGC Part Numbers	Function
100000042	4-Bit Shift Register
100000012	4-Bit Shift Register
100000134	4-Bit Data Selector/Storage Register
100000137	8-Bit Position Scaler
100000085	4-By-4 Register File
100000135) 100000234)	4-Bit Bidirectional Universal Shift Register
100000101	8-Bit Shift Register
100000111) 100000109) 100000125)	Buffer Registers
100000112	Dual 8-Bit Shift Register
100000151	Hex 40-Bit Static Shift Register
100000152	1024-Bit Recirculating Dynamic Shift Register
100000171	16-Bit Multiple-Port Register File With 3-State Outputs
100000180	High-Speed 4-Bit Shift Register With Enable
100000510	8-Bit Parallel-In Serial-Out Shift Register
100000362	8-Bit Parallel-Out Serial-In Shift Register
100000511	8-Bit Serial-In Parallel-Out Shift Register
100000367	4-By-4 Register Files W/3-State Outputs
100000381	Dynamic Shift Register
100000383) 100000504)	Dual 2-Wide 2-Input AND-OR-INVERT Gates
100000389	Parallel-Load 8-Bit Shift Register
100000390	Quadruple 2-Input Positive-NAND Gate W/Open-Collector Outputs
100000436	Dual 144-Bit Mask Programmable Static Shift Register
100000541	8-Bit Parallel-Out Shift Register
100000542	Parallel-Load 8-Bit Shift Register

DG-02045

SPECIAL FUNCTIONS

DGC Part Number	Function
100000136	Eight-Input Priority Encoder
100000002	16 Diode Array
100000131	General Purpose Transistor Array
100000193	Timer
100000127	Zero Voltage Switch

DG-02046

VOLTAGE REGULATORS

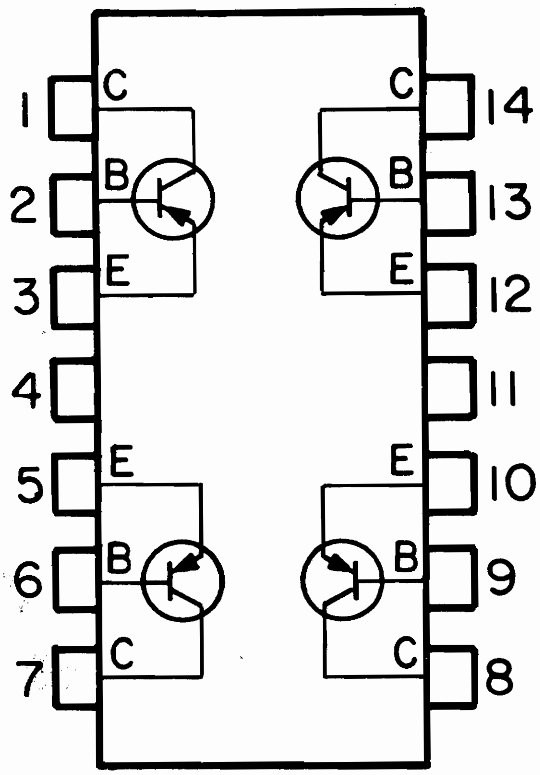
DGC Part Number	Function
100000026) 100000094) 100000318)	Precision Voltage Regulator
100000290	Three-Terminal Negative Regulator
100000359) 100000380)	Positive Voltage Regulators
100000355	Three-Terminal Positive Regulator
100000484	Three-Terminal Negative Regulator

DG-02047

100000001

PNP Quad Core Driver

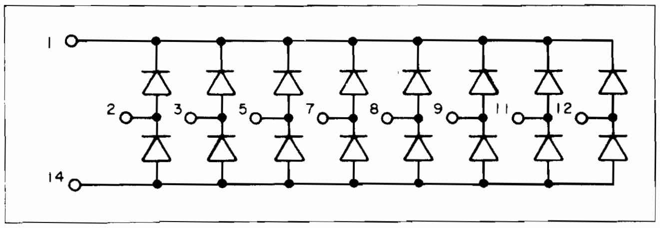
Pin Configuration



100000002

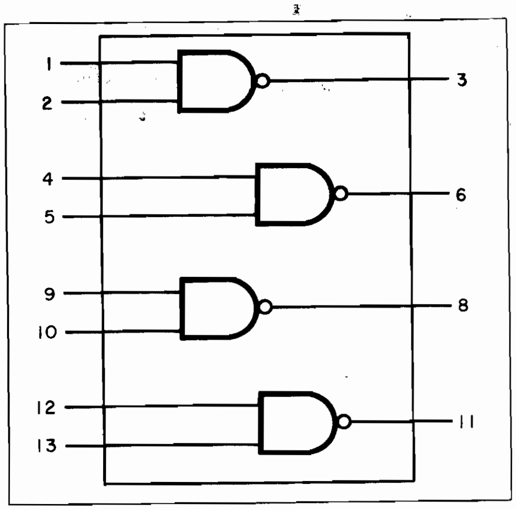
16 Diode Array

Logic Diagram



100000003

Pin Configuration



Quad 2-Input NAND Gate

Logic Diagram/Pin Designations

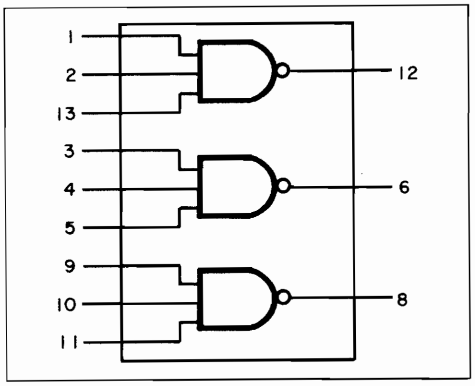
V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

All Inputs High = Low Out
Any Input Low = High Out

100000004

Pin Configuration



Triple 3-Input NAND Gate

Logic Diagram/Pin Designations

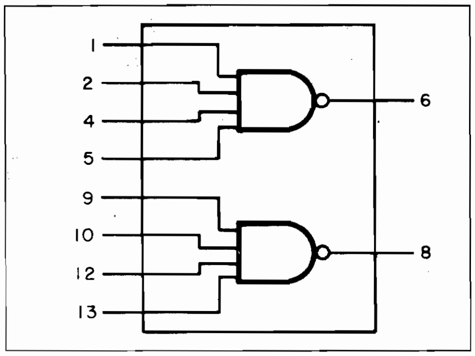
V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

All Inputs High = Low Out
Any Input Low = High Out

100000005 100000009 100000040

Pin Configuration



Dual 4-Input NAND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

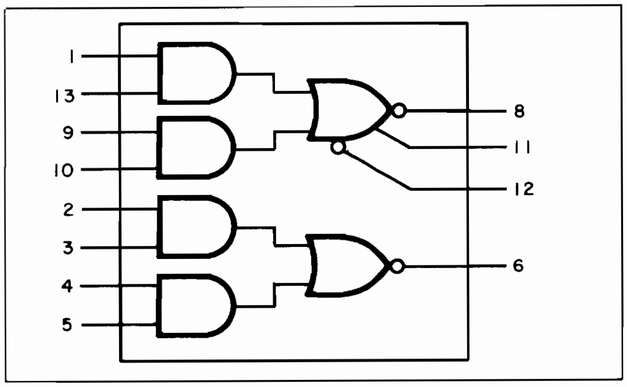
Truth Table

All Inputs High = Low Out
Any Input Low = High Out

The 100000009 device has higher input-output loading parameters than 100000005.

100000006

Logic Diagram



Dual Extendable AND-OR-INVERT Gates

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

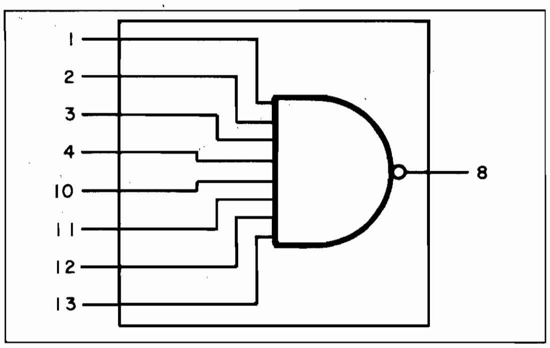
Truth Table

$(2 \cdot 3) \cdot (4 \cdot 5) = \overline{6}$
$(\overline{2} + \overline{3}) + (\overline{4} + \overline{5}) = 6$

Four extenders may be tied to these terminals.

100000007

Logic Diagram



8 - Input NAND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

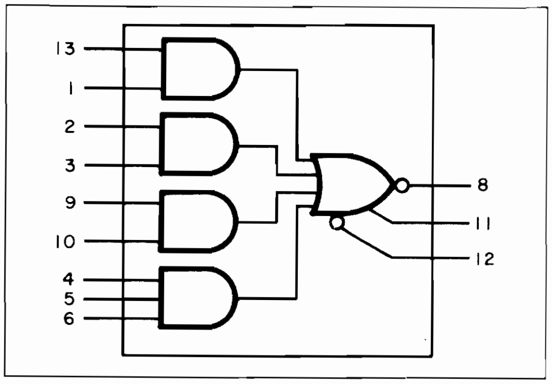
Truth Table

All Inputs High = Low Out

Any Input Low = High Out

100000008

Pin Configuration



Single Extendable AND-OR-INVERT Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

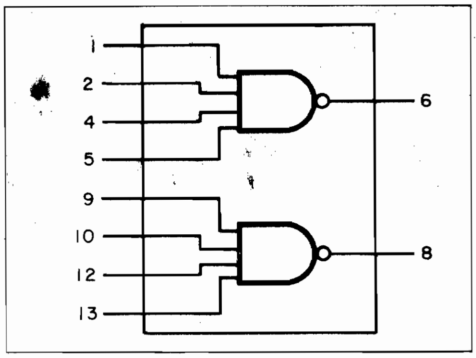
$(1 \cdot 13) \cdot (2 \cdot 3) \cdot (9 \cdot 10) \cdot (4 \cdot 5 \cdot 6) = \overline{8}$

$(1 + 13) + (2 + 3) + (9 + 10) + (4 + 5 + 6) = 8$

Four extenders (100000039) may be tied to these terminals.

100000005 100000009 100000040

Pin Configuration



Dual 4-Input NAND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

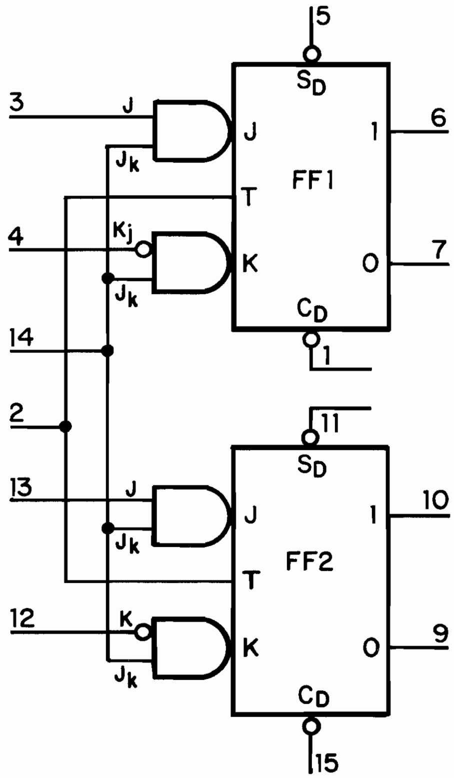
Truth Table

All Inputs High = Low Out
Any Input Low = High Out

The 100000009 device has higher input-output loading parameters than 100000005.

100000011

Functional Block Diagram



Dual J-K Flip-Flop

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Truth Tables

Synchronous Operation

Before Clock Outputs One	Before Clock Outputs Zero	Inputs J	Inputs K	After Clock Outputs One	After Clock Outputs Zero
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

Asynchronous Operation

Inputs S_D	Inputs C_D	Outputs One	Outputs Zero
L	L	H	H
L	H	H	L
H	L	L	H
H	H	Synchronous Inputs Control	

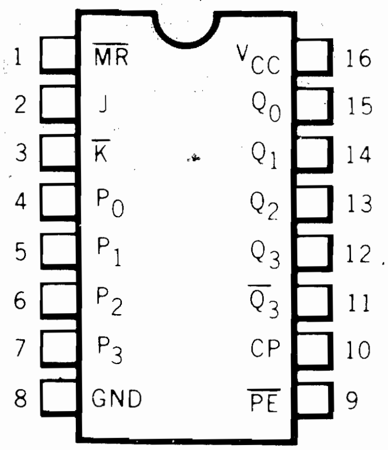
Synchronous Operation: The truth table defines the next state of the flip-flop after a Low to High transition of the clock pulse. The next state is a function of the present state and the J and K inputs as shown in the table.

The L* symbol means that input does not go High at any time while the clock is Low. The H* symbol means that the input is High at some time while the clock is Low. The X symbol indicates that the condition of that input has no effect on the next state of the flip-flop. The H and L symbols refer to steady state High and Low voltage levels, respectively.

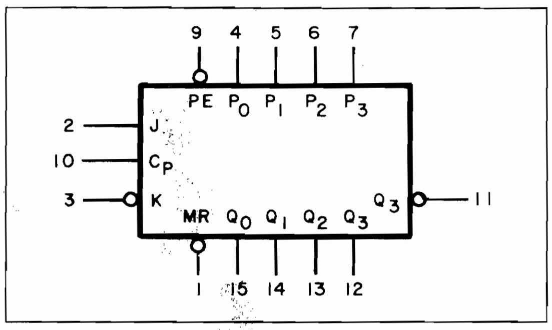
100000012

4-Bit Shift Register

Pin Configuration



Logic Symbol



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Nomenclature

$\overline{PE}$	Parallel Enable (Active Low) Input
P_0, P_1, P_2, P_3	Parallel Inputs
J	First Stage J (Active High) Input
$\overline{K}$	First Stage K (Active Low) Input
Cp	Clock Active High Going Edge Input
$\overline{MR}$	Master Reset (Active Low) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
$\overline{Q_3}$	Complementary Last Stage Output

Truth Table
For Serial Entry

J	$\overline{K}$	Q_o at $t_{(n+1)}$
L	L	L
L	H	Q_o at t_n (no change)
H	L	$\overline{Q}_o$ at t_n (toggles)
H	H	H

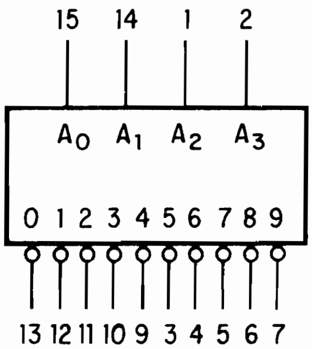
$\overline{PE}$ = High, $\overline{MR}$ = High, (n+1) indicates state after next clock.

Data entry is synchronous with the registers changing state after each low to high transition of the clock. With the parallel enable low, the parallel inputs determine the next condition of the shift register. When the parallel enable input is high the shift register performs a one-bit shift to the right, with data entering the first stage flip-flop through $\overline{JK}$ inputs. By tying the two inputs together D type entry is obtained.

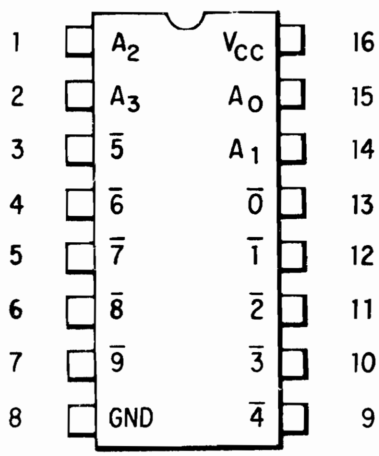
The asynchronous active low master reset when activated overrides all other input conditions and clears the register.

100000013

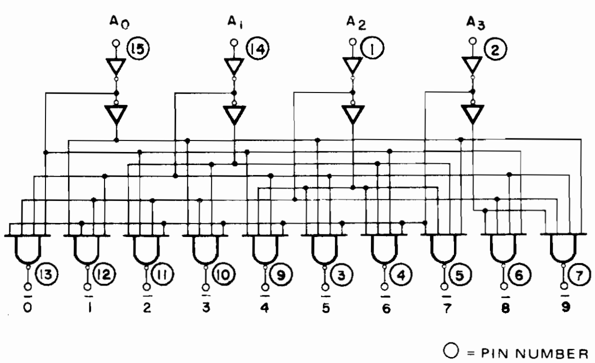
Logic Symbol



Pin Configuration



Logic Diagram



One-Of-Ten Decoder

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

A_0, A_1, A_2, A_3 = Addressed Inputs

$\overline{0}$ to $\overline{9}$ = Outputs, Active LOW

Truth Table

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

The 100000013 is a multipurpose decoder designed to accept four active HIGH BCD inputs and to provide ten mutually exclusive active LOW outputs, as shown by the logic symbol.

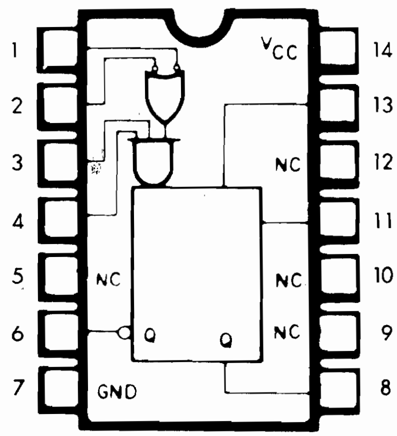
The logic design ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant A_3 input produces a useful inhibit function when the device is used as a one-of-eight decoder.

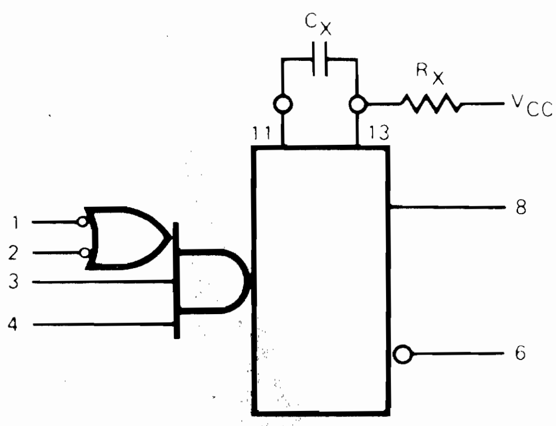
100000015

Retriggerable Monostable Multivibrator

Pin Configuration



Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Triggering Truth Table

Pin Numbers				
1	2	3	4	Operation
H→L	H	H	H	Trigger
H	H→L	H	H	Trigger
L	X	L→H	H	Trigger
X	L	L→H	H	Trigger
L	X	H	L→H	Trigger
X	L	H	L→H	Trigger

T (trigger) = $(\overline{1} + \overline{2}) \cdot 3 \cdot 4$

Change of T from FALSE to TRUE causes trigger.

H = HIGH voltage level $\geqslant V_{IH}$

L = LOW voltage $\leqslant V_{IL}$

L→H = transition from LOW to HIGH voltage level

H→L = transition from HIGH to LOW voltage level

X = Don't care (either HIGH or LOW voltage level)

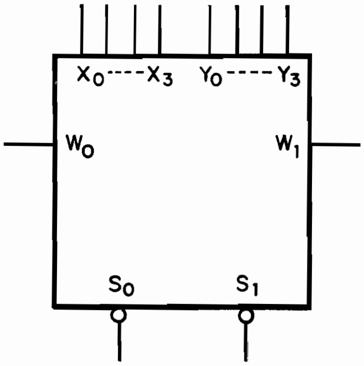
This retriggerable monostable multivibrator provides an output pulse whose duration and accuracy is a function of external timing components.

This device has four inputs, two active HIGH and two active LOW. This allows a choice of leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the device and result in a continuous true output. Retriggering may be inhibited by tying the negation (Q) output to an active LOW input. Active pullups are provided on the outputs for good drive capability into capacitive loads.

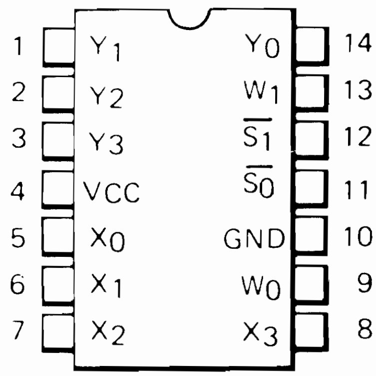
100000016

16-Bit Coincident Select Read-Write Memory

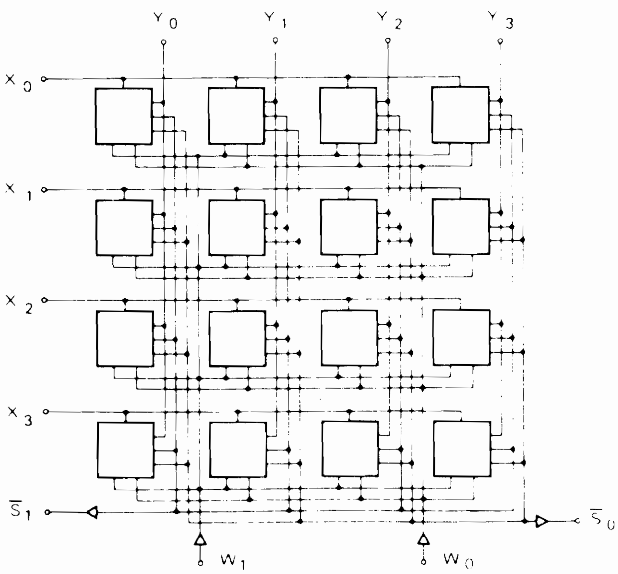
Logic Symbol



Pin Configuration



Logic Diagram



Each square represents one bit of storage.

X,Y – Address
W – Write Input
S – Sense Output

Logic Diagram/Pin Designations

V_{CC} = Pin 4
Gnd = Pin 10

This device is comprised of 16-bit, bit-oriented, non-destructive readout memory cells. These memory cells, organized as 16 words by one bit, are designed for high speed scratch-pad memory applications.

The memory cell consists of 16 RS flip-flops arranged in an addressable four-by-four matrix. The desired bit location is selected by raising the coincident X-Y address lines to a logic "H" level (>2.1 volts) and holding the non-selected address lines at logic "L" level (<0.7 volts). As many as four locations may be addressed simultaneously without destroying stored information. The stored data and its complement at the addressed bit location may be read at the output terminals. If the addressed bit location contains a "1", the $\overline{S_1}$ output will be LOW and the $\overline{S_0}$ output will be HIGH. If the addressed bit location contains a "0", the $\overline{S_1}$ output will be HIGH and the $\overline{S_0}$ output will be LOW.

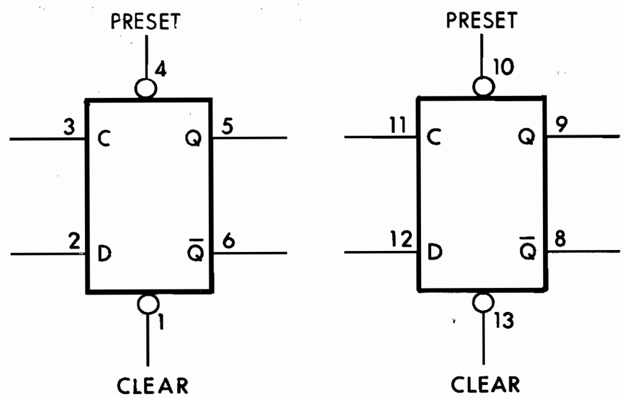
Writing is accomplished by activating one of the write amplifiers. To write a "1", the desired bit location is addressed and the input of the "write one" (W_1) amplifier is raised to a HIGH level. To write a "0", the input of the "write zero" (W_0) amplifier is raised to a HIGH level.

The outputs are open-collector, which may be wired OR for word expansion. (The output transistors are off when none of the bits are selected.) An external resistor should be returned to V_{CC} to pull-up the wired OR outputs.

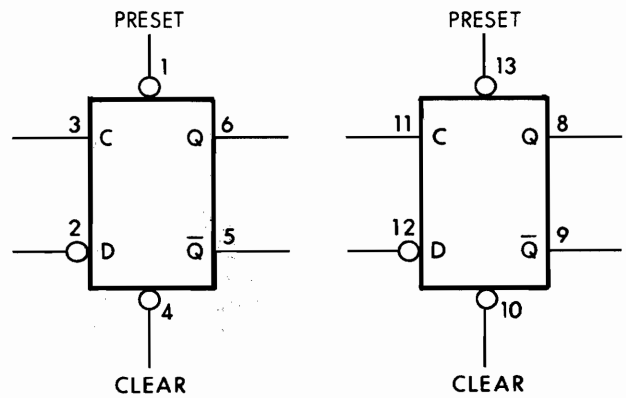
100000017 100000257 100000300

Dual D-Type Edge-Triggered Flip-Flop

Pin Connections



Alternate Pin Connections



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Function Table

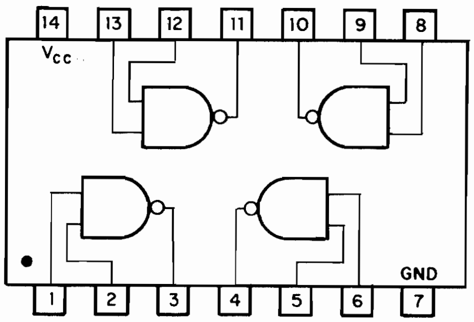
Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Note: The 100000300 is a Schottky device.

100000019

Pin Configuration



Quad 2-Input NAND Interface Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

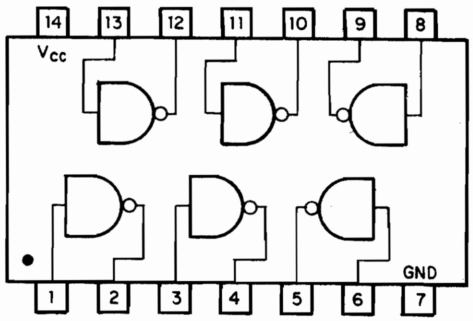
Truth Table

V_{IN}	V_{IN}	V_{OUT}
L	L	H
L	H	H
H	L	H
H	H	L

100000020 100000071

Hex Inverter

Pin Configuration



Logic Diagram/Pin Designations

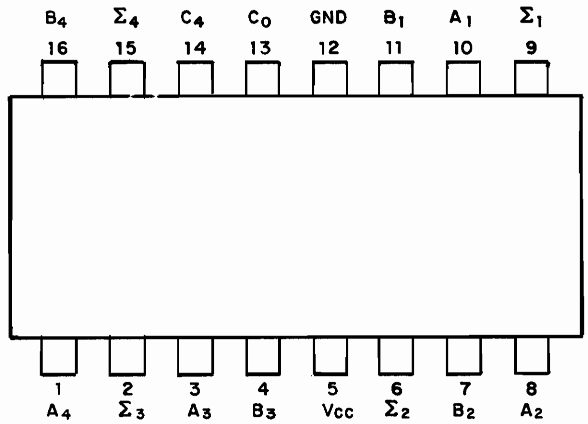
V_{CC} = Pin 14

Gnd = Pin 7

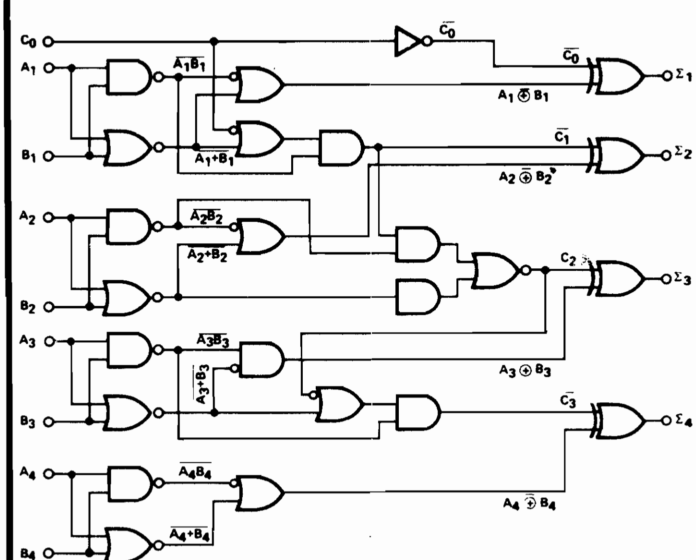
100000021

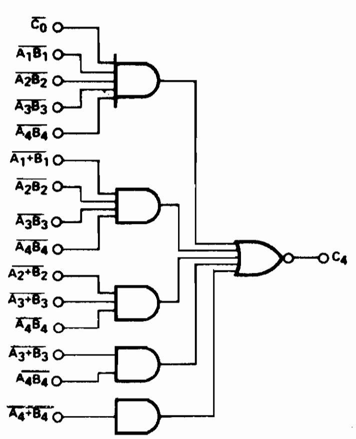
4-Bit Binary Full Adder (Look Ahead Carry)

Pin Configuration



Logic Diagrams





Logic Diagram/Pin Designations

V_{CC} = Pin 5

Gnd = Pin 12

Truth Table

INPUT				OUTPUT					
				WHEN $C_0 = 0$ / WHEN $C_2 = 0$			WHEN $C_0 = 1$ / WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Note:

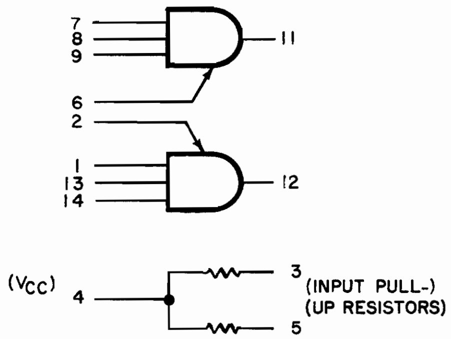
Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4 and B_4 are then used to determine outputs Σ_3, Σ_4 and C_4.

The 100000021 is a 4-Bit Binary Full Adder for adding two four bit binary numbers. A Carry Look Ahead circuit is included to provide minimum carry propagation delays.

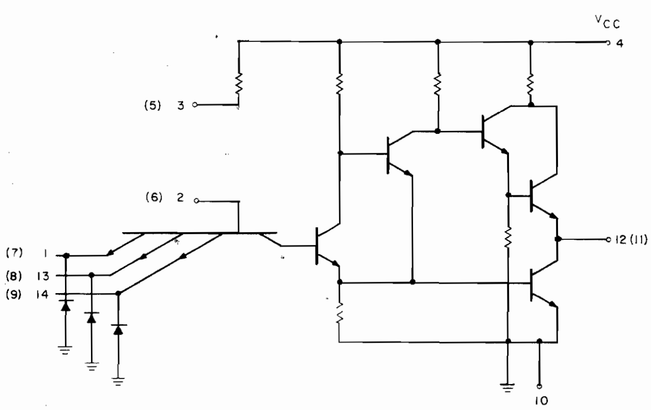
100000023 100000356 100000357

Dual Pulse Shaper-Delay AND Gate

Logic Diagram



Schematic

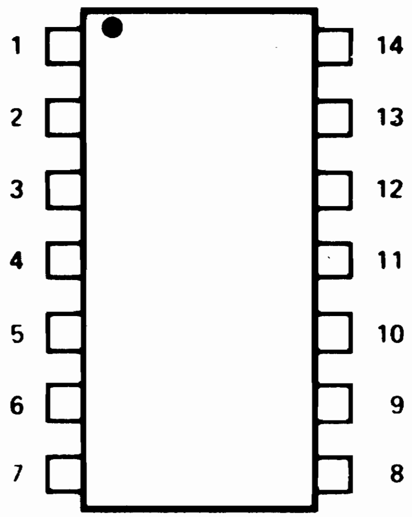


REV. 03

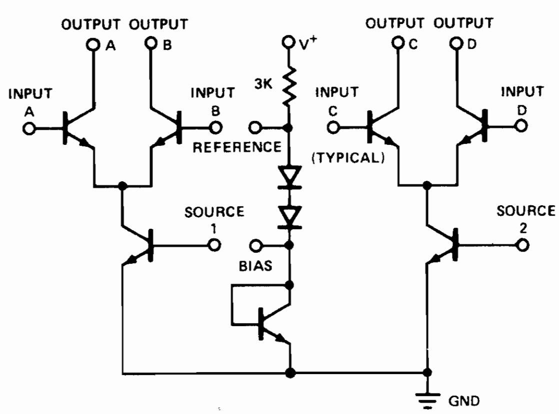
100000024

Dual Differential Amplifier

Pin Configuration



Basic Circuit Schematic



Pin Designations

1.	Output B	8.	Source 2
2.	Output A	9.	Bias
3.	Input A	10.	Input D
4.	Input B	11.	Input C
5.	Reference	12.	Output C
6.	Source 1	13.	Output D
7.	Ground	14.	V+

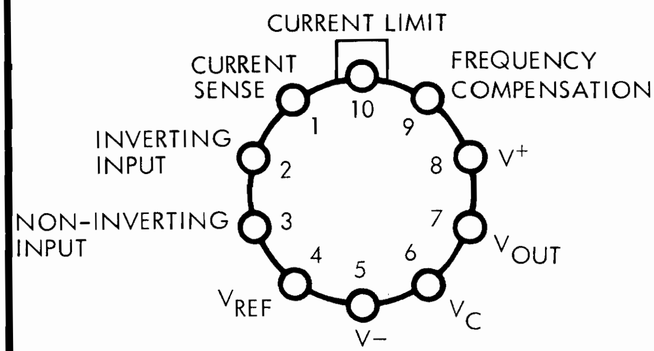
The 100000024 is a dual high-frequency differential amplifier with associated constant current sources and biasing elements contained within a silicon monolithic epitaxial substrate. This device is intended for RF-IF amplifier service to beyond 100mHz. Circuit layout provides for connection as either a high-gain, common-emitter, common-base, cascade amplifier or a common-collector, common-base, differential amplifier. Automatic gain control may be applied to either circuit.

100000026 10000094 100000318

Precision Voltage Regulator

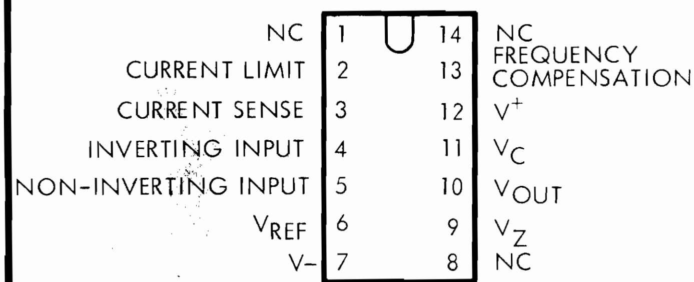
The 100000026(Can) and 100000094,100000318(DIP) are monolithic voltage regulators, consisting of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150mA are required. Provisions are made for adjustable current limiting and remote shutdown.

Pin Configurations



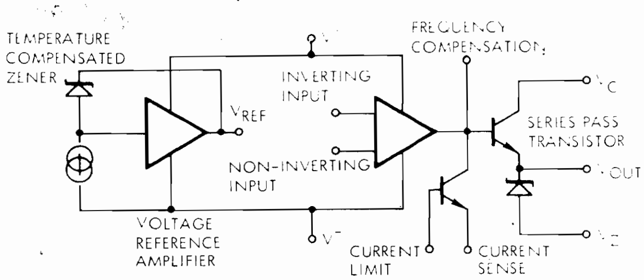
Note: pin 5 is connected to case

100000026



100000094

Equivalent Circuit



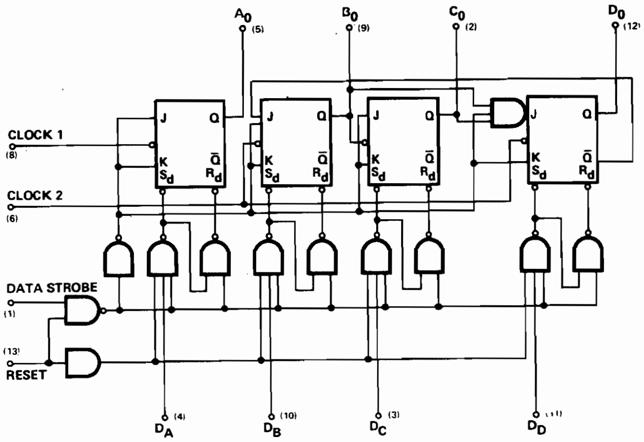
REV. 03

100000038 100000028

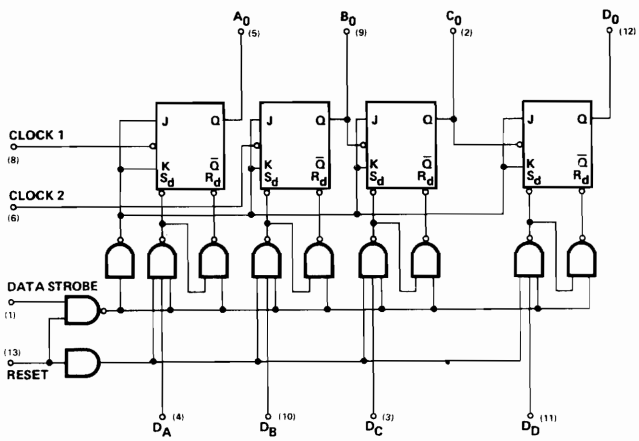
BCD Decade Counter/Storage Element
4-Bit Binary Counter/Storage Element

Logic Diagrams

100000038



100000028



Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

The 100000038 Decade Counter and the 100000028 16-State Binary Counter are four-bit subsystems.

The Decade Counter can be connected in the BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode.

The Binary Counter may be connected as a divide-by-two, eight, or sixteen counter.

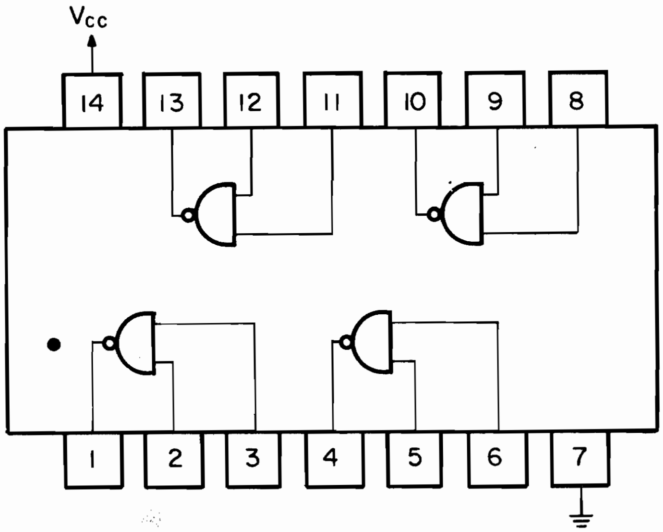
Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level.

Both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse; however, there is no restriction on the transition time since the individual binaries are level-sensitive.

100000036

Pin Configuration



Quad 2-Input NAND Gate

Logic Diagram/Pin Designations

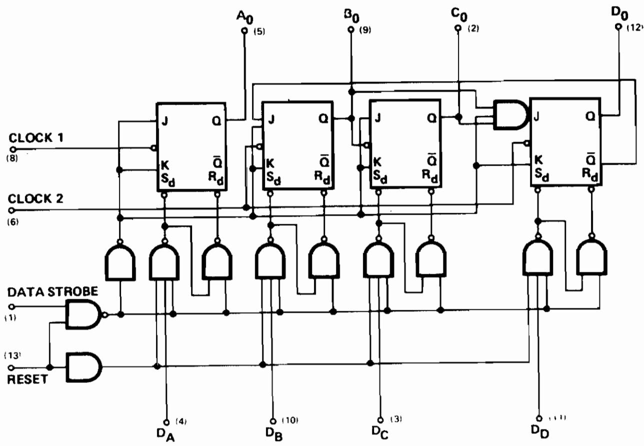
V_{CC} = Pin 14

Gnd = Pin 7

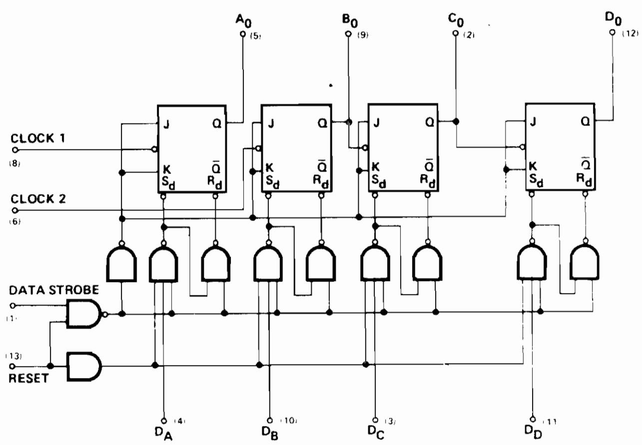
100000038 100000028

Logic Diagrams

100000038



100000028



BCD Decade Counter/Storage Element
4-Bit Binary Counter/Storage Element

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

The 100000038 Decade Counter and the 100000028 16-State Binary Counter are four-bit subsystems.

The Decade Counter can be connected in the BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode.

The Binary Counter may be connected as a divide-by-two, eight, or sixteen counter.

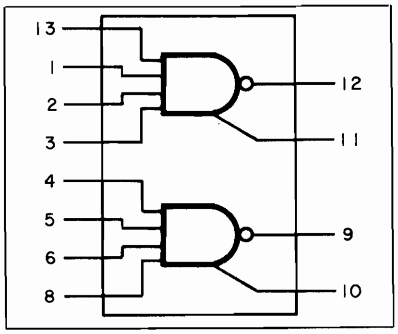
Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level.

Both units are provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse; however, there is no restriction on the transition time since the individual binaries are level-sensitive.

100000039

Logic Diagram



Dual Extender AND-OR-INVERT Gates

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

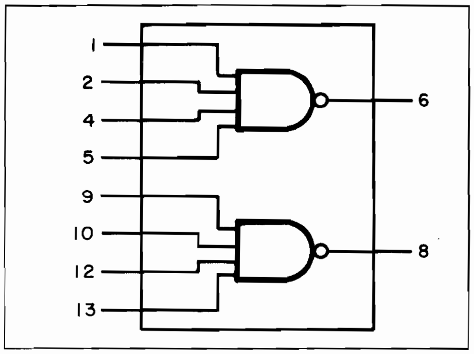
$4 \cdot 5 \cdot 6 \cdot 8 = \overline{9}$
$\overline{4} + \overline{5} + \overline{6} + \overline{8} = 9$

Extender for use with 100000006 and 100000008.

100000005 100000009 100000040

Dual 4-Input NAND Gate

Pin Configuration



Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

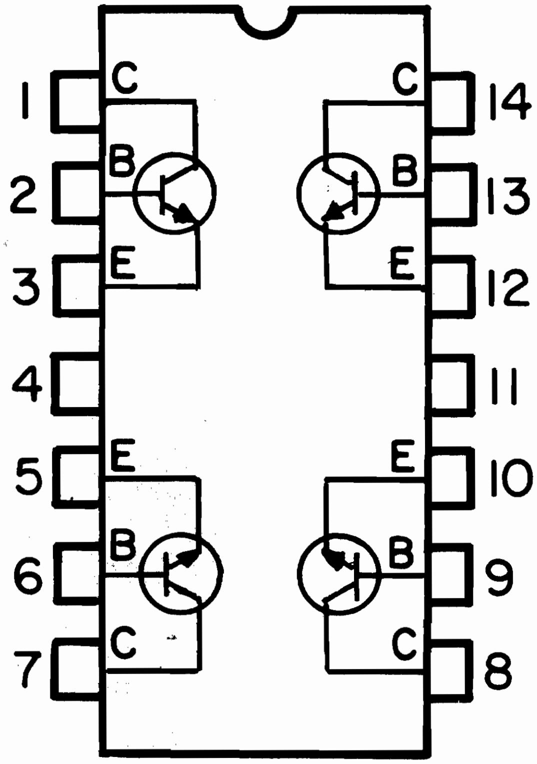
All Inputs High = Low Out
Any Input Low = High Out

The 100000009 device has higher input-output loading parameters than 100000005.

100000041

NPN Quad Core Driver

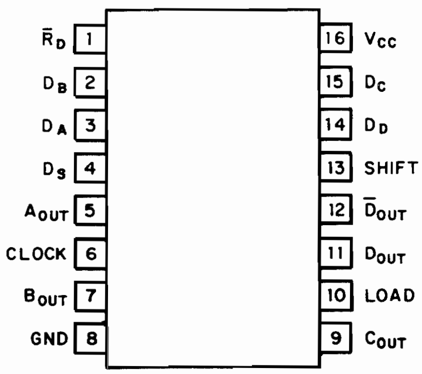
Pin Configuration



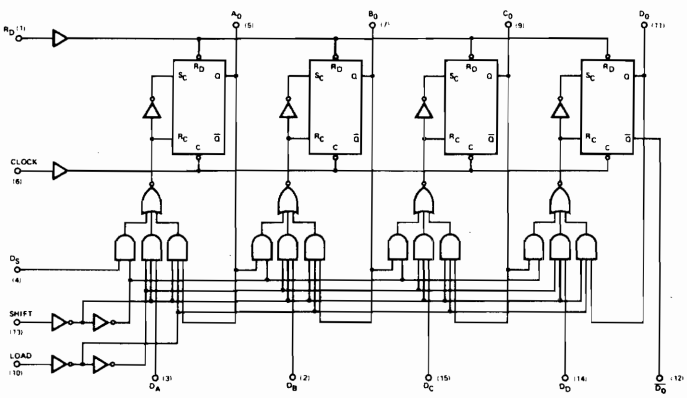
100000042

4-Bit Shift Register

Pin Configuration



Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Truth Table

Control State	Load	Shift
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

This 4-bit shift register has both a serial and a parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

This device provides a direct reset ($\overline{R_D}$) and a $\overline{D_{out}}$ line.

The internal design uses level sensitive binaries which respond to the negative-going clock transition. A buffer clock driver is included to minimize input clock loading.

Mode control logic is available to determine three possible control states. These register states are serial shift right mode, parallel enter mode, and no change or hold mode. These states accomplish logical decoding for system control. The control modes are shown in the truth table.

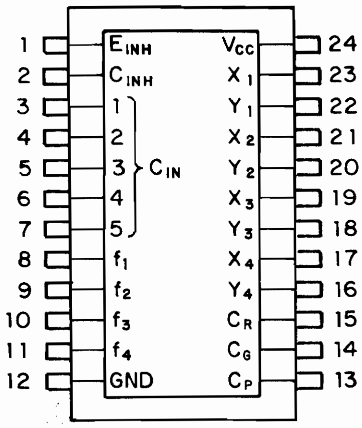
For applications not requiring the hold mode, the load input may be tied high and the shift input used as the mode control.

Note: The 100000520 is a Schottky device.

100000043

Arithmetic Logic Element

Pin Configuration



Logic Diagram/Pin Designations

V_{CC} = Pin 24

Gnd = Pin 12

Truth Table

$C_{INH} = 1 \rightarrow A_n = 1$

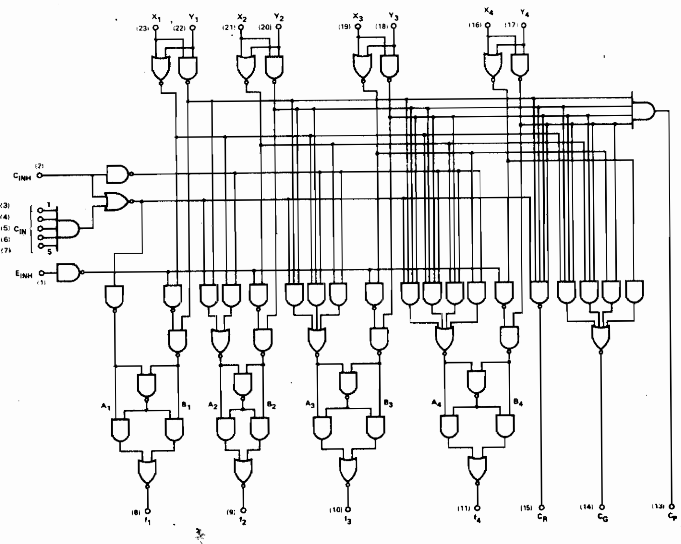
$C_{INH} = 0 \rightarrow A_n =$

C_{IN}	A_1	A_1	X_1	Y_1	A_2	A_2	X_2	Y_2	A_3	A_3	X_3	Y_3	A_4
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	1	0	0	0	1	0
		0	1	0	0	0	1	0	0	0	1	0	0
		0	1	1	1	0	1	1	1	0	1	1	1
		1	0	0	0	1	0	0	0	1	0	0	0
		1	0	1	1	1	0	1	1	1	0	1	1
		1	1	0	1	1	1	0	1	1	1	0	1
		1	1	1	1	1	1	1	1	1	1	1	1

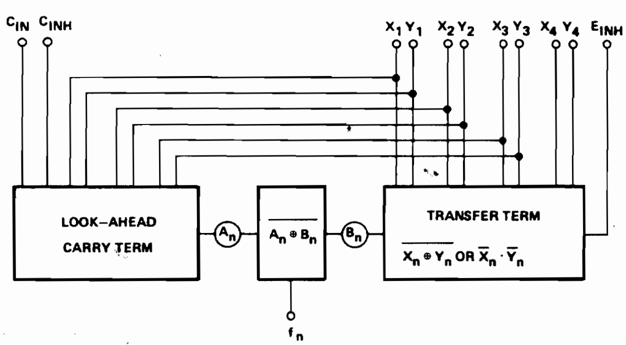
A_n	B_n	f_n
0	0	1
0	1	0
1	0	0
1	1	1

E_{INH}	X_n	Y_n	B_n
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Logic Diagram



Functional Block Diagram



This arithmetic logic element is a monolithic gate array incorporating four full-adders structured in a look-ahead mode. The device may be used as four mutually independent exclusive NOR or AND gates by proper addressing of the inhibit lines.

As a four-bit adder, this device permits high speed parallel addition of four sets of data and has both simultaneous addition on a character to character and on a bit to bit basis.

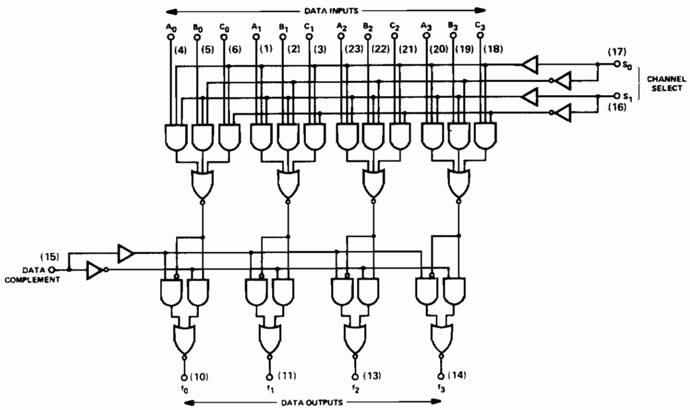
When true input variables are used, the true sum is formed at the f output. Inverted input variables produce the complement of the sum of the true variables.

The carry-outs available are: Internally Generated (C_G), Propagated (C_p) and Ripple (C_R).

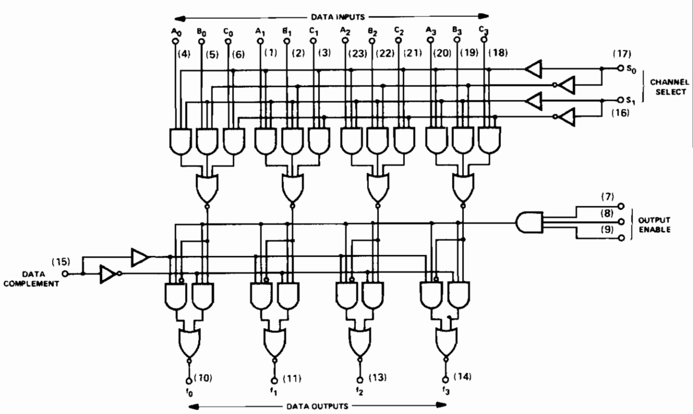
100000129 100000044

Logic Diagrams

100000129
(Active Pull-up)



100000044
(Open Collector)



3-Input, 4-Bit Digital Multiplexer

Logic Diagram/Pin Designations

V_{CC} = Pin 24
Gnd = Pin 12

Truth Table

Data Input A_n B_n C_n	Channel Select S_0 S_1	Data Complement	Output Enable '044	Data Outputs
A_n x x	1 1	0	1	A_n
x B_n x	0 1	0	1	B_n
x x C_n	1 0	0	1	C_n
x x x	0 0	0	1	0
A_n x x	1 1	1	1	$\overline{A_n}$
x B_n x	0 1	1	1	$\overline{B_n}$
x x C_n	1 0	1	1	$\overline{C_n}$
x x x	0 0	1	1	1
x x x	x x	x	0	1

X = Either state.

The 3-input, 4-bit multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

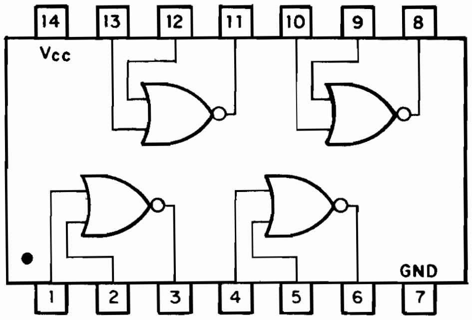
The data complement input controls the conditional complement circuit at the multiplexer output to effect either inverting or non-inverting data flow.

The 100000129 employs active output structures to effect minimum delays; the 100000044 utilizes bare collector outputs for expansion of input terms.

The 100000044 may be expanded by connecting its outputs to the outputs of another 100000044. Provision is made for use of a 3-bit code to determine which multiplexer is selected; thus, eight multiplexers may be commoned to effect a 4-pole, 24-position switch.

100000045

Pin Configuration



Quad 2-Input NOR Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

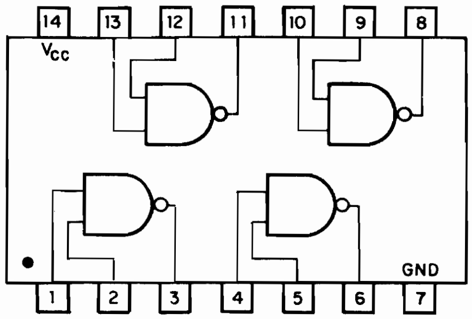
Gnd = Pin 7

Truth Table

V_{IN}	V_{IN}	V_{OUT}
H	H	L
H	L	L
L	H	L
L	L	H

100000046

Pin Configuration



Quad 2-Input NAND Gate

Logic Diagram/Pin Designations

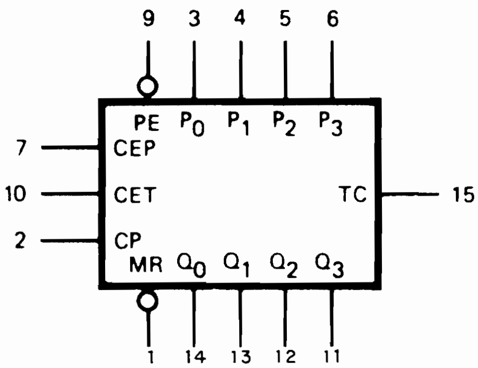
V_{CC} = Pin 14

Gnd = Pin 7

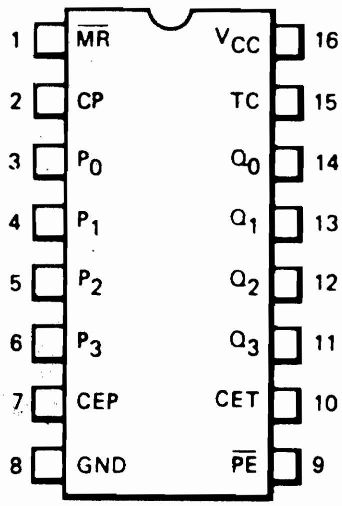
100000153 100000047

BCD Decade Counter-4 Bit Binary Counter

Logic Symbol

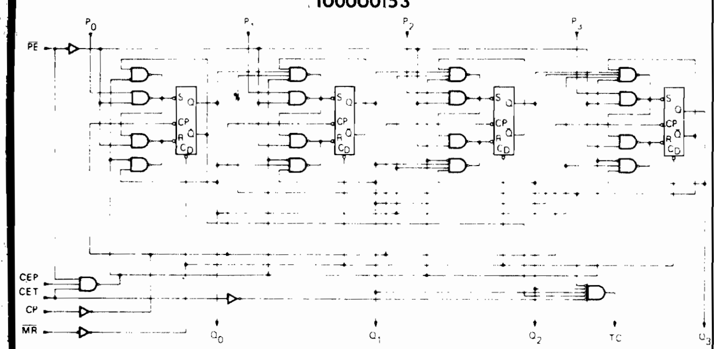


Pin Configuration

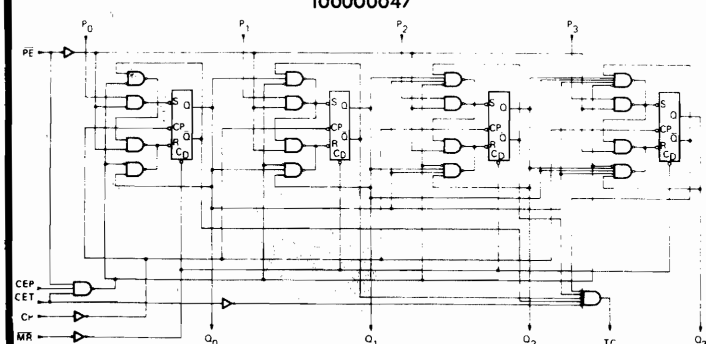


Logic Diagrams

100000153



100000047



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

$\overline{PE}$.............. Parallel Enable (Active LOW) Input

P_0, P_1, P_2, P_3.. Parallel Inputs

CEP .... Count Enable Parallel Input

CET .... Count Enable Trickle Input

CP.............. Clock (Active HIGH Going Edge) Input

$\overline{MR}$ .... Master Reset (Active LOW) Input

Q_0, Q_1, Q_2, Q_3.. Parallel Outputs

TC.............. Terminal Count Outputs

Mode Selection

$\overline{PE}$	CEP	CET	Mode
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH)

Terminal Count Generation

CET	100000153 ($Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3$)	100000047 ($Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$)	TC
L	L	L	L
L	H	H	L
H	L	L	L
H	H	H	H

$TC = CET \cdot Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3$ (100000153)

$TC = CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$ (100000047)

Positive Logic:

H = HIGH Voltage Level
L = LOW Voltage Level

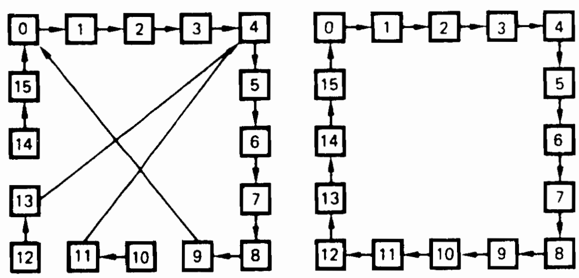
The 100000153 is a high speed BCD decade counter, and the 100000047 is a high speed binary counter. Both counters are fully synchronous with the clock pulse driving four master/slave flip-flops in parallel through a clock buffer. During the

Continued ...

100000153 100000047

Continued

100000153 100000047



Logic Equations

Count Enable = CEP · CET · PE
TC for 100000153 = CET · Q_0 · $\overline{Q_1}$ · $\overline{Q_2}$ · Q_3
TC for 100000047 = CET · Q_0 · Q_1 · Q_2 · Q_3
Preset = $\overline{PE}$ · CP + (rising clock edge)
Reset = $\overline{MR}$

Note: The 100000153 can be preset to any state but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

LOW to HIGH transition of the clock, the master is inhibited from further change. After the masters are locked out, data is transferred from the master to the slaves and reflected at the outputs. When the clock is HIGH, the masters are inhibited and the master/slave data path remains established. During the HIGH to LOW transition of the clock, the slave is inhibited from further change, followed by the enabling of the masters for the acceptance of data from the counting logic or the parallel entry logic.

The three control inputs, Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP), and Count Enable Trickle (CET), select the mode of operation. When the conditions for counting are satisfied, the rising edge of a clock pulse will change the counters to the next state of the count sequence shown in the State Diagram. The Count Mode is enabled when CEP and CET inputs and $\overline{PE}$ are HIGH.

These devices can be synchronously preset from the four Parallel inputs (P_{0-3}) when $\overline{PE}$ is LOW. When the Parallel Enable and Clock are LOW, each master of the flip-flops is connected to the appropriate parallel input (P_{0-3}) and the slaves (outputs) are steady in their previous state. When the clock goes HIGH, the masters are inhibited and this information is transferred to the slaves and reflected at the outputs. The parallel enable input overrides both count enable inputs, presetting the counter when LOW.

Terminal count is HIGH when the counter is at terminal count (state 9 for 100000153 and state 15 for 100000047), and Count Enable Trickle is HIGH, as shown in the logic equations.

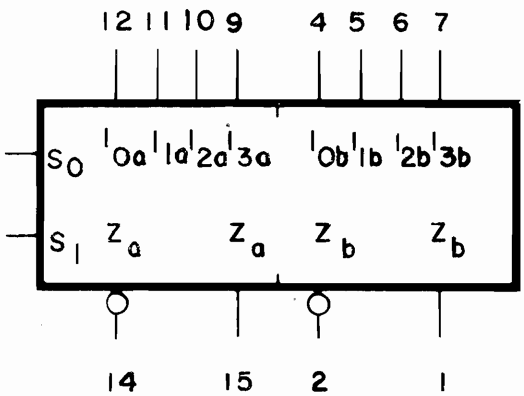
When LOW, the asynchronous master reset overrides all other inputs resetting the four outputs LOW.

Conventional operation, as shown in the Mode Selection table, requires that the mode control inputs ($\overline{PE}$, CEP, CET) are stable while the clock is LOW.

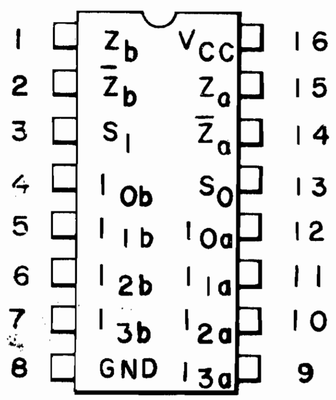
100000048

Dual Four-Input Multiplexer

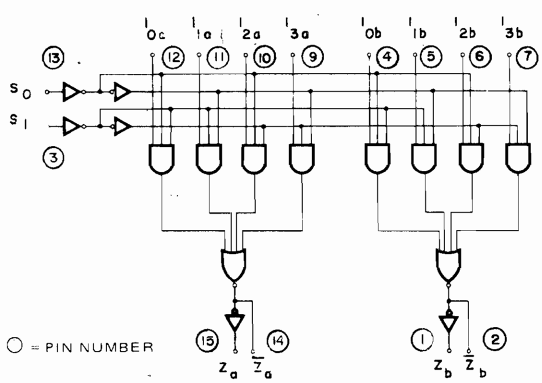
Logic Symbol



Pin Configuration



Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

S_0, S_1 .... Common Select Inputs

Multiplexer A

I_{0a}, I_{1a}, I_{2a}, I_{3a} .. Multiplexer Inputs

Z_a.................. Multiplexer Output

$\overline{Z}_a$.................. Complementary Multiplexer Output

Multiplexer B

I_{0b}, I_{1b}, I_{2b}, I_{3b} ... Multiplexer Inputs

Z_b.................. Multiplexer Output

$\overline{Z}_b$.................. Complementary Multiplexer Output

Truth Table

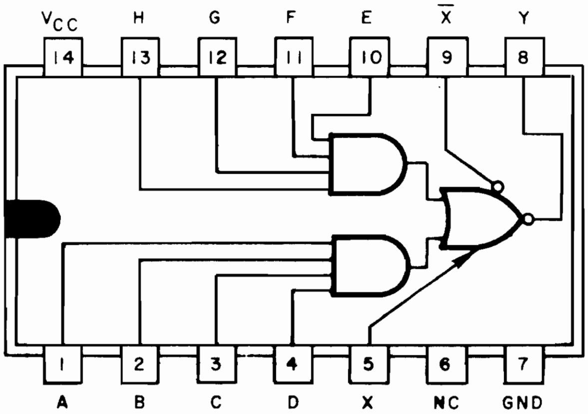
Select Inputs		Inputs				Outputs	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	$\overline{Z}_a$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	$\overline{Z}_b$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Either HIGH or LOW Logic Level

The 100000048 is a monolithic, high speed, Dual Four-Input Multiplexer circuit, consisting of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. This device can generate any two functions of three variables. It may be cascaded to multiple levels so that any number of lines can be multiplexed on to a single output bus.

100000049

Pin Configuration



Expandable 4-Input AND-OR-INVERT Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

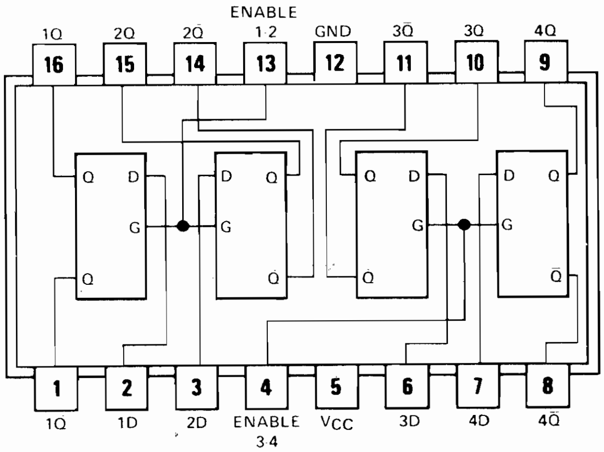
Gnd = Pin 7

Both expander inputs are used simultaneously for expanding. If expander is not used, leave X and $\overline{X}$ pins open.

Positive logic: $Y = (ABCD) + (EFGH) + (X)$

100000050 100000387

Pin Configuration



4-Bit Bistable Latches

Logic Diagram/Pin Designations

V_{CC} = Pin 5

Gnd = Pin 12

Function Table
(Each Latch)

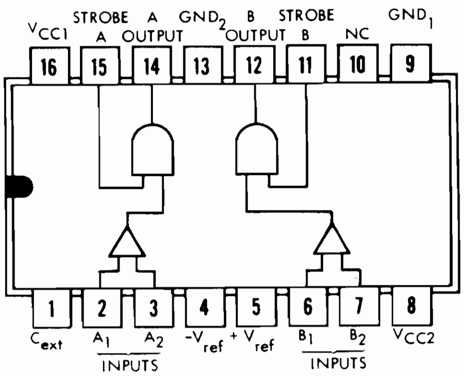
Inputs D	Inputs G	Ouputs Q	Ouputs $\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level; L = low level; X = irrelevant.
Q_0 = the level of Q before the high-to-low transition of G.

These latches are suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

100000052

Pin Configuration



Dual Sense Amplifier

Logic Diagram/Pin Designations

V_{CC1} = Pin 16

V_{CC2} = Pin 8

Gnd 1 = Pin 9

Gnd 2 = Pin 13

Truth Table

$IN_A \cdot$ STROBE A = OUT A
$\overline{IN_A} \cdot$ STROBE A = $\overline{\text{OUT A}}$
$IN_B \cdot$ STROBE B = OUT B
$\overline{IN_B} \cdot$ STROBE B = $\overline{\text{OUT B}}$

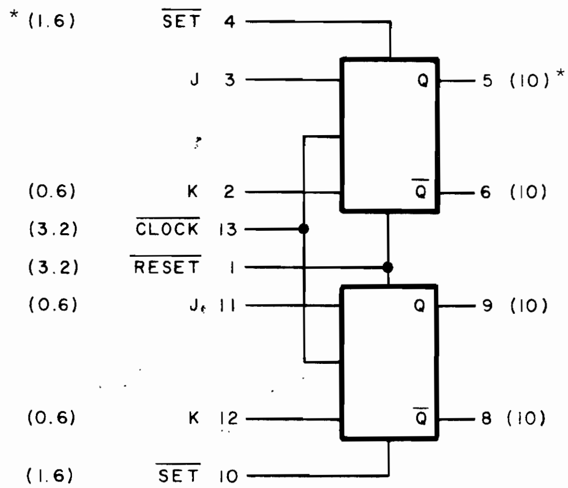
100000053

Dual J-K Flip-Flop

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Logic Diagram



*Loading Max. Shown in Parenthesis

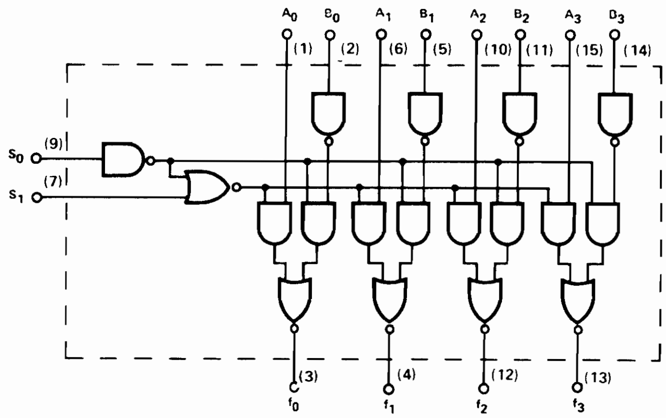
Truth Table

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

100000057 100000108

2-Input, 4-Bit Digital Multiplexer

Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Truth Table

Select Lines		Outputs
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	1

The 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing TTL circuit structures. The 100000108 features a bare-collector output to allow expansion with other devices.

The multiplexer is able to choose from two different input sources, each containing 4 bits: A = (A_0, A_1, A_2, A_3); B = (B_0, B_1, B_2, B_3). The selection is controlled by the input S_0, while the second control input, S_1, is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with added elements to perform Addition/Subtraction. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

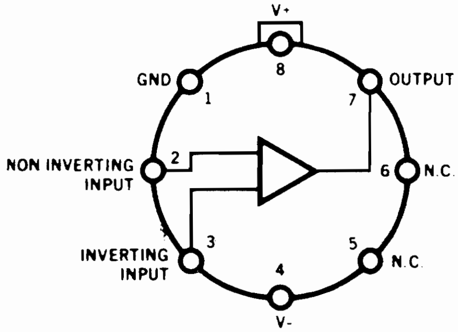
100000059 100000157 100000324

High-Speed Differential Comparator

The 100000059, 100000324(CAN) and 100000157(DIP) are differential voltage comparators intended for applications requiring high accuracy and fact response times. Constructed on a single silicon chip, the devices are useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high-noise immunity line receiver.

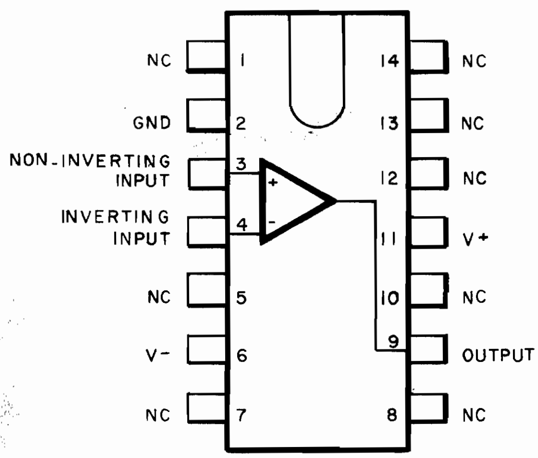
Pin Configurations

100000059, 100000324



Note: Pin 4 connected to case.

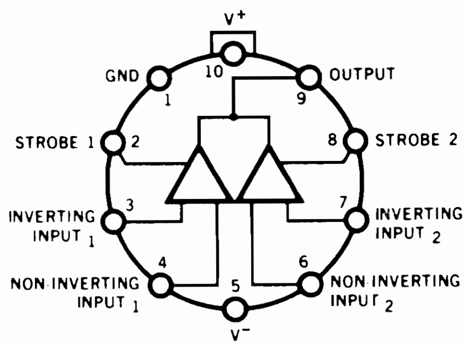
100000157



100000060 100000343

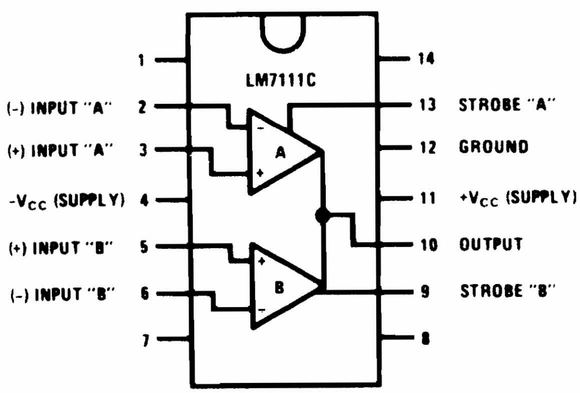
Dual Comparator

Pin Configuration



100000060

Dual-In-Line Package



100000343

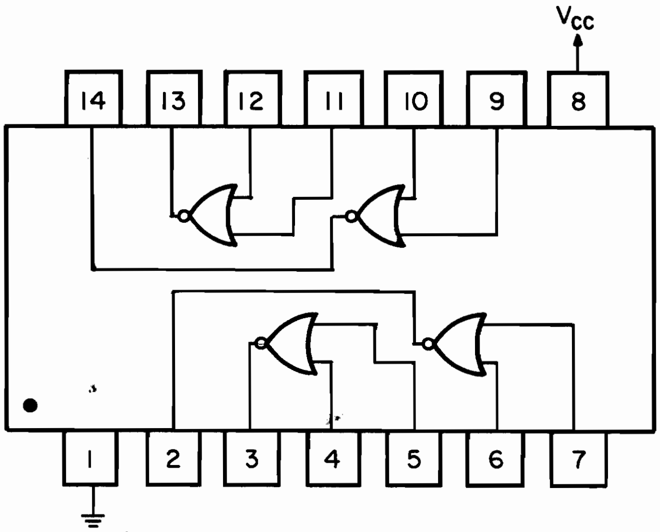
This device is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms.

When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided.

100000061

Quad 2-Input NOR Gate

Pin Configuration



Logic Diagram/Pin Designations

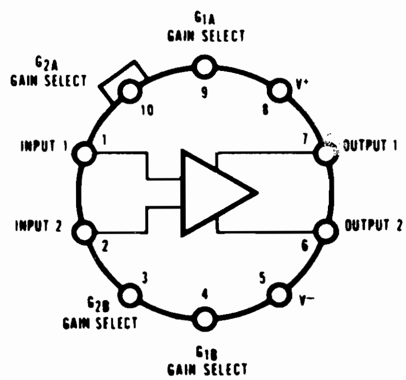
V_{CC} = Pin 8

Gnd = Pin 1

100000062 100000314
100000326 100000372

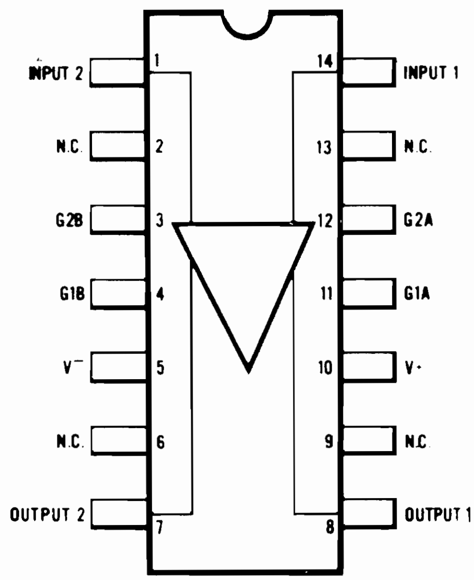
Pin Configuration

Top View



100000062, 100000326

TO-116 DUAL IN-LINE



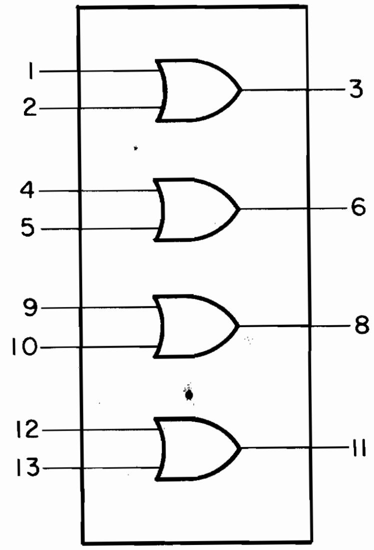
100000314, 100000372

Differential Video Amplifier

This device is a monolithic two-stage differential input, differential output video amplifier. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. This device provides fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option.

100000063

Pin Configuration



Quad 2-Input OR Gate

Logic Diagram/Pin Designations

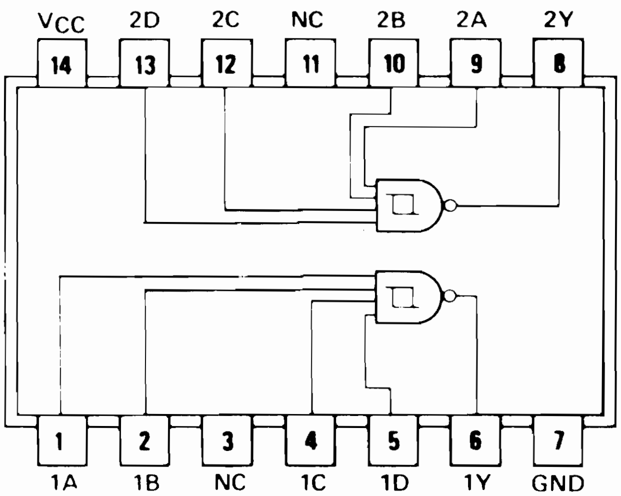
V_{CC} = Pin 14

Gnd = Pin 7

3 = 1 + 2

100000066

Pin Configuration



Dual 4-Input Positive-NAND Schmitt Trigger

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

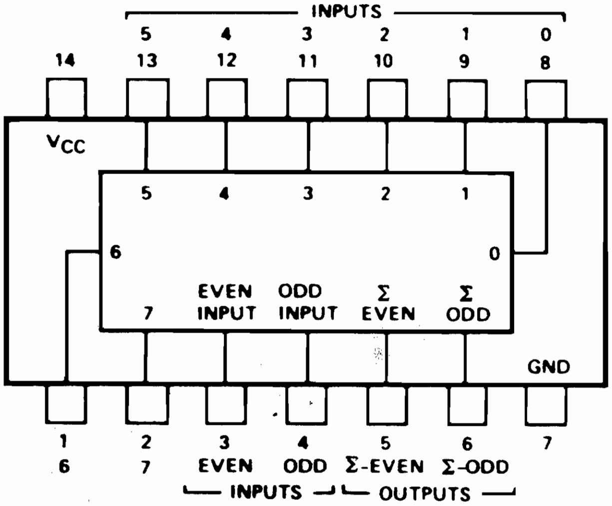
NC = No internal connection

Positive logic: $Y = \overline{ABCD}$

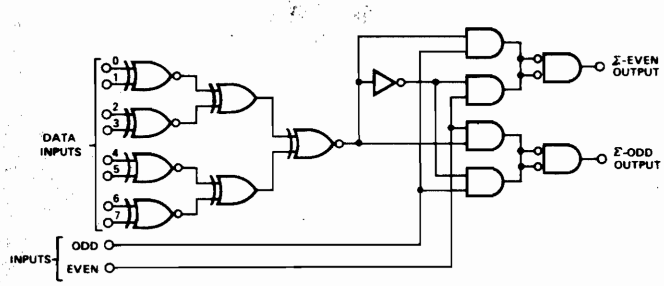
100000067

8-Bit Odd/Even Parity Generator/Checker

Pin Configuration



Logic Diagram



Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

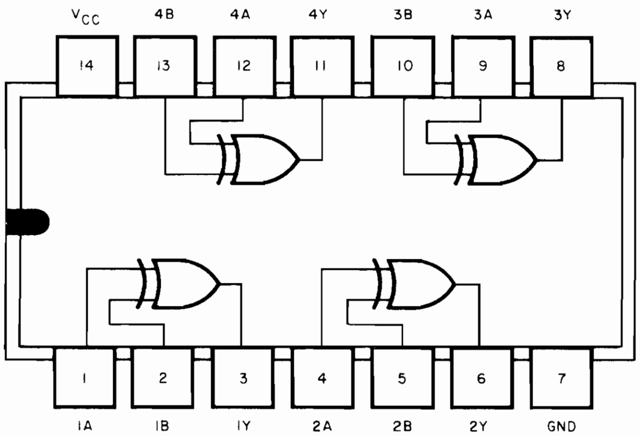
Truth Table

Inputs			Outputs	
Σof 1's at 0 thru 7	Even	Odd	Σ Even	Σ Odd
Even	1	0	1	0
Odd	1	0	0	1
Even	0	1	0	1
Odd	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant.

100000068 100000365

Pin Configuration



Quadruple 2-Input Exclusive-OR Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

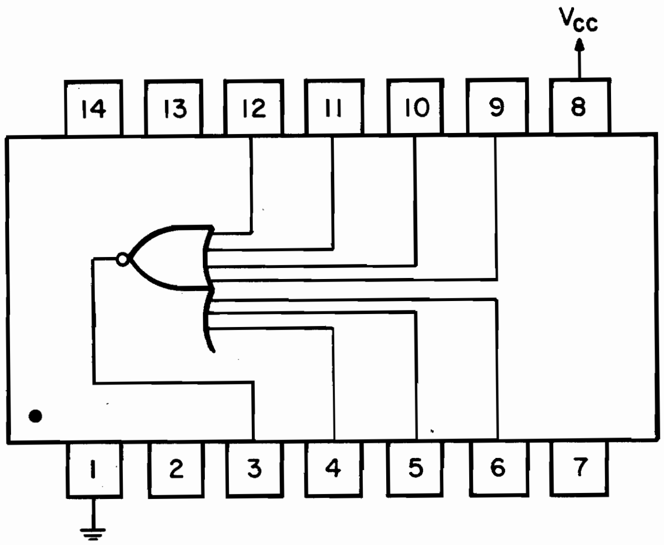
Positive logic: $Y = A \oplus B$

Note: The 100000365 is a Schottky device.

100000069

Single 7-Input NOR Gate

Pin Configuration



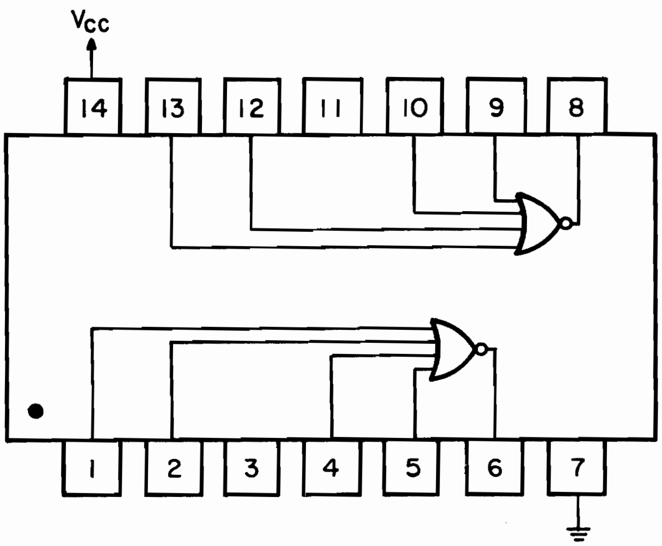
Logic Diagram/Pin Designations

V_{CC} = Pin 8

Gnd = Pin 1

100000070

Pin Configuration



Dual 4-Input NOR Gate

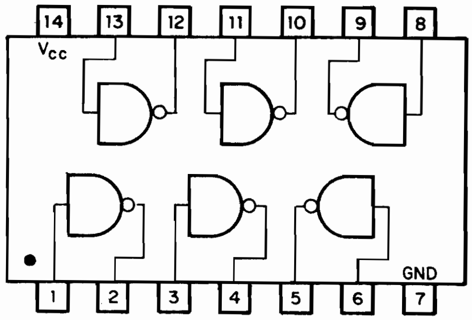
Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

100000020 100000071

Pin Configuration



Hex Inverter

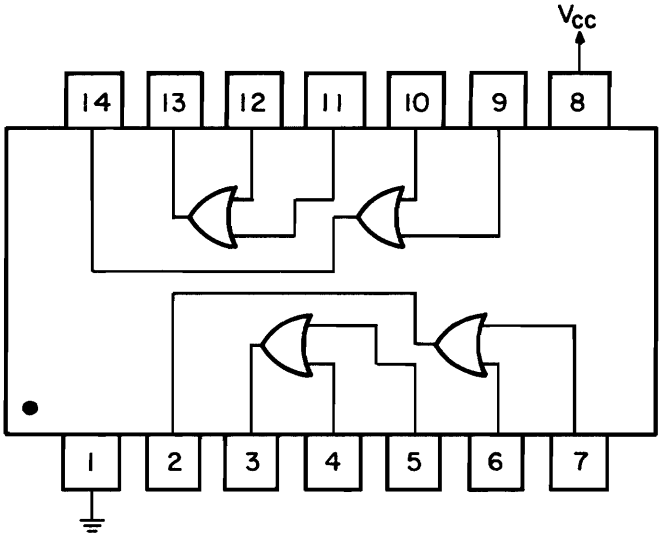
Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

100000072

Pin Configuration



Quad 2-Input OR Gate

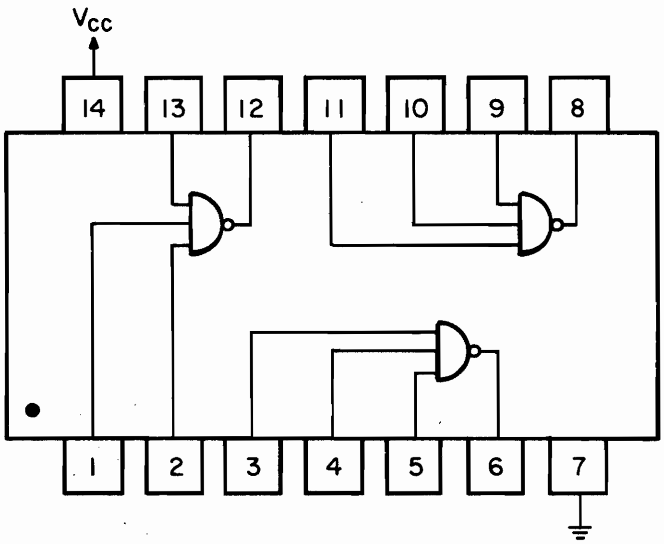
Logic Diagram/Pin Designations

V_{CC} = Pin 8
Gnd = Pin 1

100000073

Triple 3-Input NAND Gate

Pin Configuration



Logic Diagram/Pin Designations

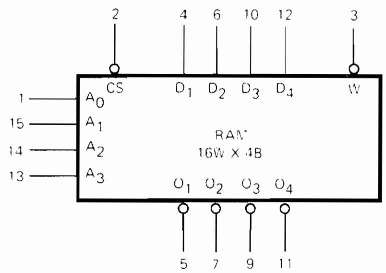
V_{CC} = Pin 14

Gnd = Pin 7

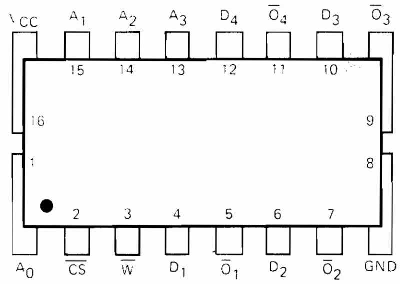
100000074

64-Bit Random Access Memory

Logic Symbol



Pin Configuration



NOTE: PIN 1 is marked for orientation.

Logic Diagram/Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{W}$	D_i	$\overline{O}_i$	
H	L	L	H	No Selection) Note
H	L	H	L	No Selection) Note
H	H	X	H	No Selection
L	L	L	H	Write "0"
L	L	H	L	Write "1"
L	H	X	$\overline{D}_i(t_{n-x})$	Read

H = HIGH Voltage Level
L = LOW Voltage Level

Note: When the chip select $\overline{CS}$ input is HIGH and the Write Enable $\overline{W}$ is LOW data is not written into the memory. However, the data outputs do follow the data inputs inverted.

The 100000074 is a 64-bit RAM, using Schottky diode clamped transistors. The memory is organized as a fully decoded 16-word memory of 4 bits per word. Memory expansion is provided by an active LOW Chip Select ($\overline{CS}$) input and open collector OR tieable outputs. Chip selection for large memory systems can be controlled by active LOW output decoders.

An active LOW Write line ($\overline{W}$) controls the writing/reading operation of the memory. When the Chip Select and Write lines are LOW the information on the four Data Inputs, D_1 to D_4, is written into the addressed memory word.

Reading is performed with the Chip Select line LOW and the Write line HIGH. The information stored in the addressed word is read out on the four inverting inputs, $\overline{O}_1$ to $\overline{O}_4$.

Whenever the write enable is LOW the four outputs of the memory follow the four data input lines inverted.

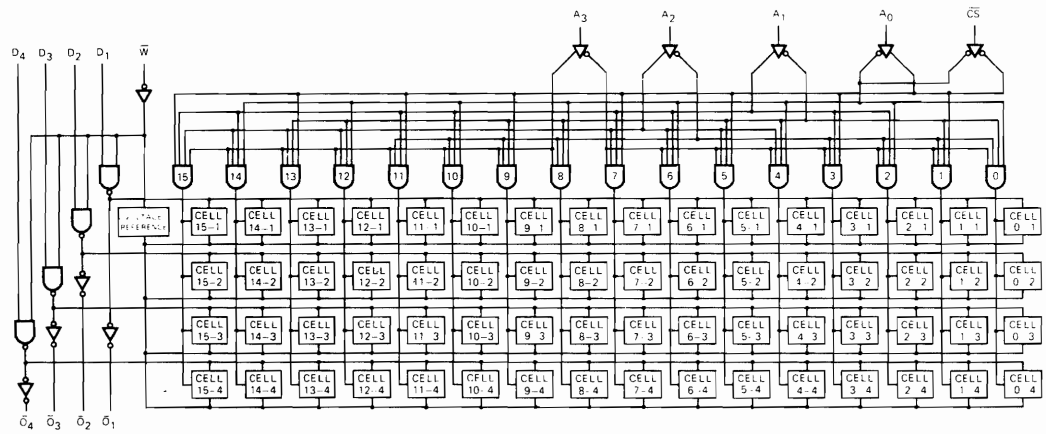
Any time the chip select is HIGH and the write enable is HIGH, all four outputs go HIGH.

Continued . . .

100000074

Continued

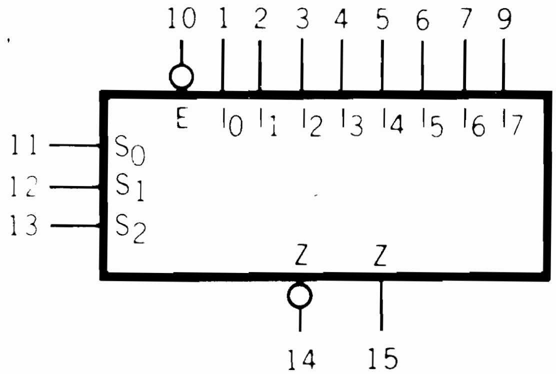
Logic Diagram



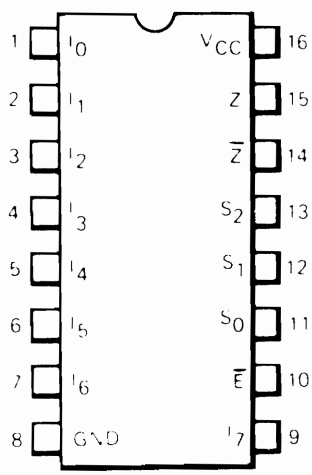
100000075

Eight-Input Multiplexer

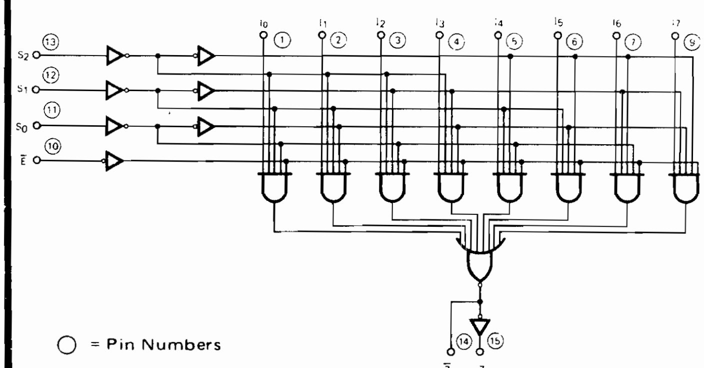
Logic Symbol



Pin Configuration



Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

S_0, S_1, S_2 ... Select Inputs
$\overline{E}$............ Enable (Active LOW) Input
I_0 to I_7 ...... Multiplexer Inputs
Z............ Multiplexer Output
$\overline{Z}$............ Complementary Multiplexer Output

Truth Table

$\overline{E}$	S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Level does not affect output.

The 100000075 is a monolithic, high speed, eight-input digital multiplexer circuit. It can be used as a universal function generator to generate any logic function of four variables. It is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select Inputs, S_0, S_1 and S_2. Both assertion and negation outputs are provided. The Enable Input ($\overline{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW, regardless of all other inputs.

Continued ....

100000075

Continued

The logic function provided at the output is:

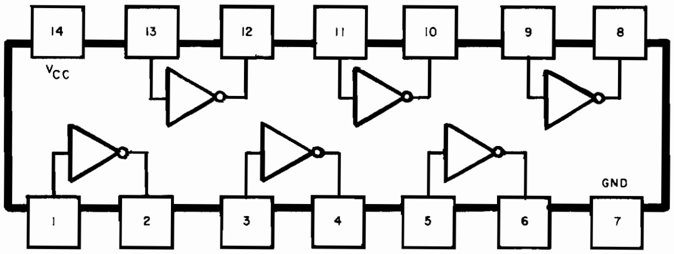
$$Z = E \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

This device provides the ability, in one package, to select from eight sources of data or control information. Proper manipulation of the inputs can provide any logic function of four variables and its negation.

100000076

Hex Inverter

Pin Configurations



Logic Diagram/Pin Designations

V_{CC} = Pin 14

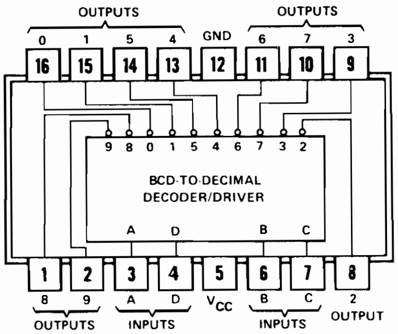
Gnd = Pin 7

Truth Table

Any Input Low	= High Out
Any Input High	= Low Out

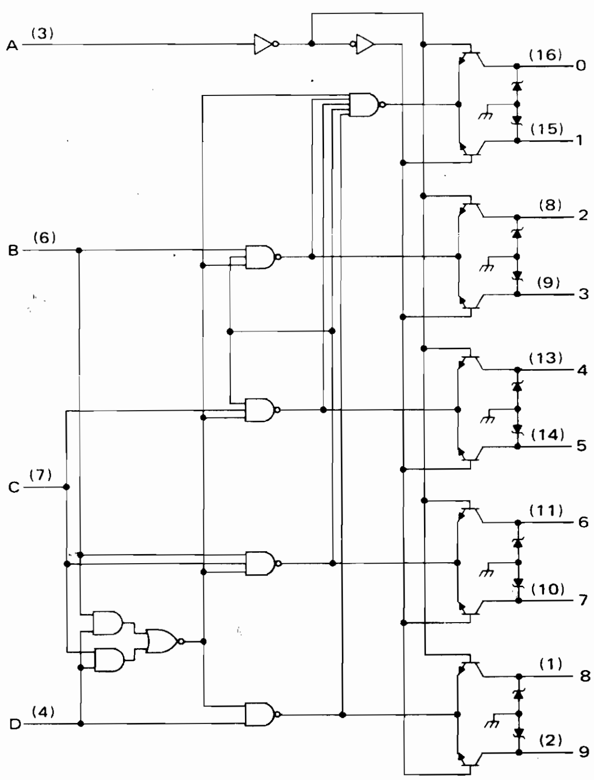
100000077

Pin Configuration



Positive Logic: See Function Table

Functional Schematic



BCD-To-Decimal Decoder-Driver

Pin Designations

V_{CC} = Pin 5

Gnd = Pin 12

Function Table

Input				Output
D	C	B	A	On*
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	None
H	L	H	H	None
H	H	L	L	None
H	H	L	H	None
H	H	H	L	None
H	H	H	H	None

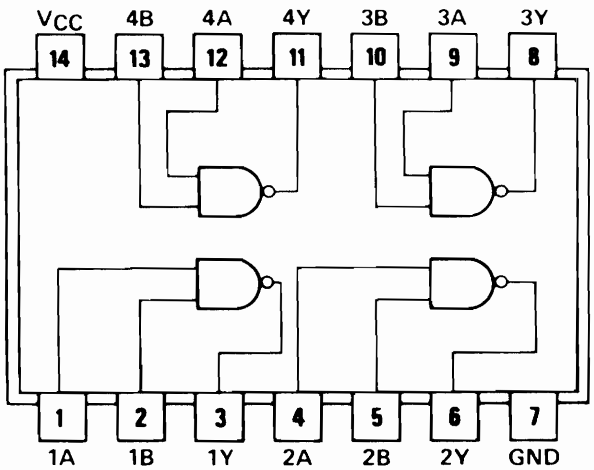
H = high level; L = low level.
* All other outputs are off.

The 100000077 is a second-generation BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore, this device, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing edge zeroes in a display. The ten high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

100000078

Pin Configuration



Quadruple 2-Input Positive-NAND Buffer With Open-Collector Outputs

Logic Diagram/Pin Designations

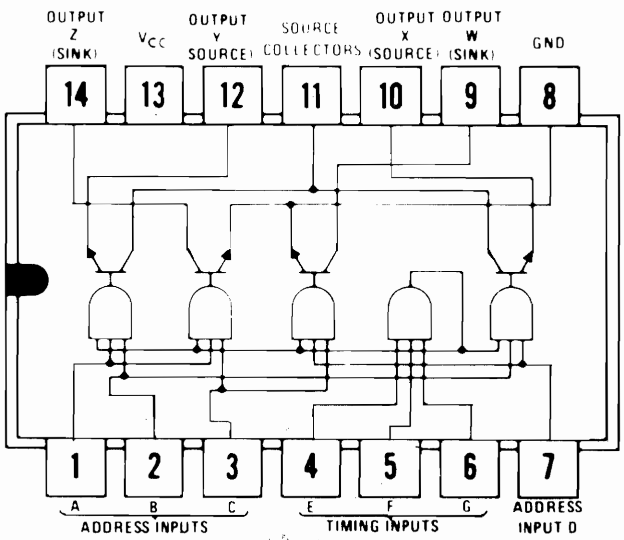
V_{CC} = Pin 14

Gnd = Pin 7

Positive logic: $Y = \overline{AB}$

100000079 100000307

Pin Configuration



Memory Driver with Decode Inputs

Logic Diagram/Pin Designations

V_{CC} = Pin 13

Gnd = Pin 8

Truth Table

Inputs							Outputs			
Address				Timing			Sink	Sources		Sink
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	On	Off	Off	Off
0	1	0	1	1	1	1	Off	On	Off	Off
1	1	0	0	1	1	1	Off	Off	On	Off
1	0	1	0	1	1	1	Off	Off	Off	On
X	X	X	X	0	X	X	Off	Off	Off	Off
X	X	X	X	X	0	X	Off	Off	Off	Off
X	X	X	X	X	X	0	Off	Off	Off	Off

Notes:

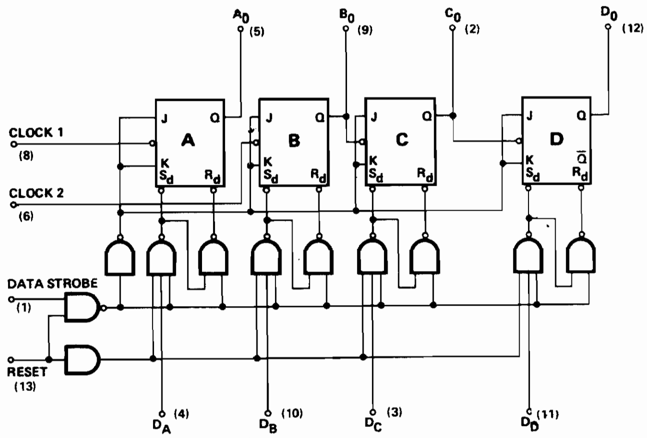
X = Logical 1 or logical 0.

Not more than one output is allowed to be On at one time: When all timing inputs are at a logical 1, two of the address inputs must be at a logical 0.

This monolithic memory driver with decode inputs is designed for use with magnetic memories. The device contains two 400 milliampere (source/sink) switch pairs, with decoding capability from four address lines. Two address inputs (B and C) are used for mode selection; i.e., source or sink. The other two address inputs (A and D) are used for switch-pair selection; i.e., output switch-pair Y/Z or W/X, respectively.

100000080 100000227

Logic Diagram



Presettable High Speed Binary Counter

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

The 100000080 Presettable High Speed Binary Counter may be connected as a divide-by-two, four, eight or sixteen counter.

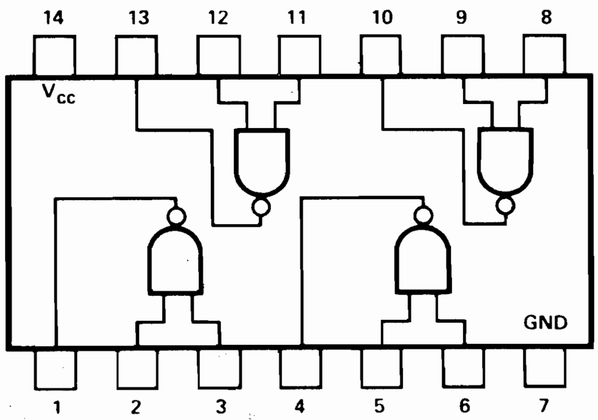
This device has strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. This unit is provided with a reset input which is common to all four bits. A "0" on the reset lines produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse.

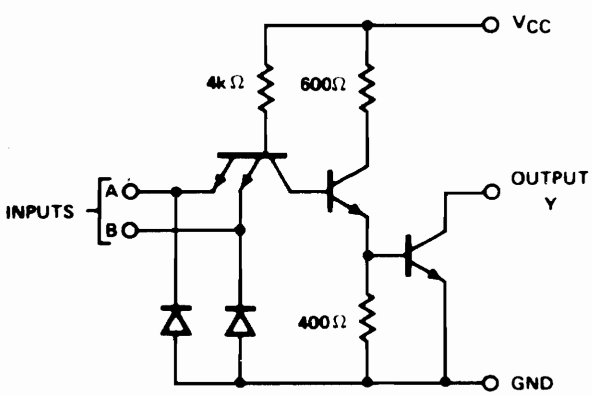
Note: The 100000227 is a Shottky device.

100000081

Pin Configuration



Schematic (Each Buffer)



Quadruple 2-Input Positive-NAND Buffer

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

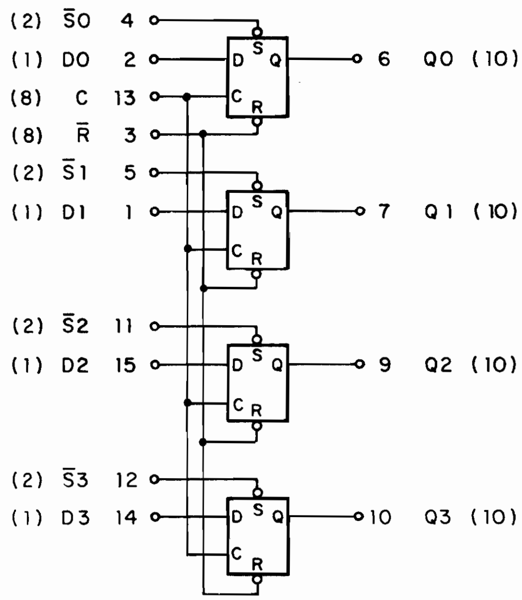
Positive logic: $Y = \overline{AB}$

The 100000081 is a NAND Gate with an open-collector output for "WIRE-AND" applications.

REV. 03

100000082

Logic Diagram



Quad D Type Flip-Flop

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Truth Table

Q	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

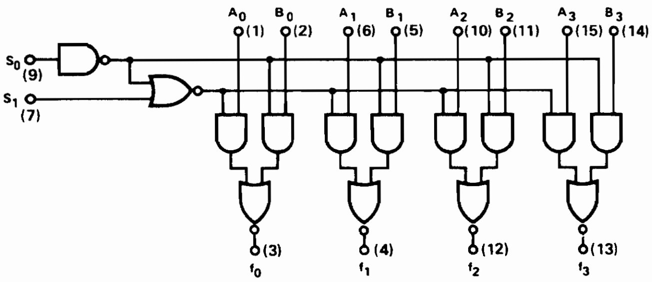
Q_{n-1} = Time period prior to clock pulse

Q_n = Time period following clock pulse

REV. 03

100000083

Logic Diagram



2-Input, 4-Bit Digital Multiplexer

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Truth Table

S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

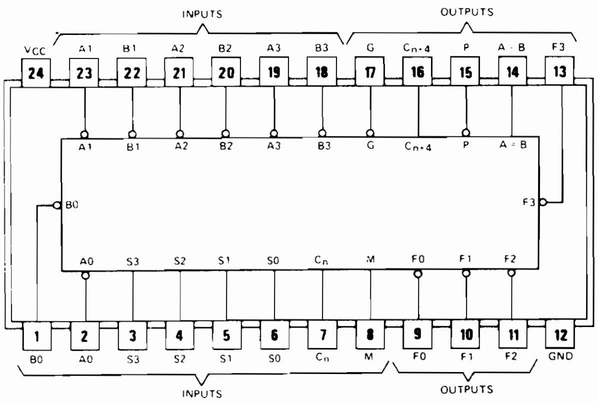
This multiplexer has inverting data paths. It has open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as one hundred four-bit words can be multiplexed by using fifty of these devices in the WIRED-AND mode.

The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

100000084 100000169 100000306

Arithmetic Logic Units/Function Generators

Pin Configuration



Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A=B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
Gnd	12	Ground

These arithmetic logic units (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip, and perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with 100000100 or 100000170, full carry look-ahead circuits, high-speed arithmetic operations can be performed. If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay is minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These devices will accommodate active-high or active-low data if the pin designations are interpreted as follows:

Continued.....

Table 1

Selection S3 S2 S1 S0	M = H Logic Functions	Active-High Data M = L: Arithmetic Operations C_n = H (no carry)	C_n = L (with carry)
L L L L	F = $\overline{A}$	F = A	F = A Plus 1
L L L H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L L H L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L L H H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L H L L	F = $\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L H L H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L H H L	F = A$\oplus$B	F = A Minus B Minus 1	F = A Minus B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H L L H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H L H H	F = AB	F = AB Minus 1	F = AB
H H L L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H H L H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H H H L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H H H H	F = A	F = A Minus 1	F = A

* Each bit is shifted to the next more significant position.

Table 2

Selection S3 S2 S1 S0	M = H Logic Functions	Active-Low Data M = L: Arithmetic Operations C_n = L (no carry)	C_n = H (with carry)
L L L L	F = $\overline{A}$	F = A Minus 1	F = A
L L L H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L L H L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L L H H	F = 1	F = Minus 1 (2's Comp)	F = Zero
L H L L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L H L H	F = $\overline{B}$	F = AB Plus (A + $\overline{B}$)	F = AB Plus (A + $\overline{B}$) Plus 1
L H H L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H L L L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H L L H	F = A$\oplus$B	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H L H H	F = A + B	F = A + B	F = (A + B) Plus 1
H H L L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H H L H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H H H L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H H H H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.

Pin No.	Active-high data Table 1	Active-low data Table 2
2	A_0	$\overline{A}_0$
1	B_0	$\overline{B}_0$
23	A_1	$\overline{A}_1$
22	B_1	$\overline{B}_1$
21	A_2	$\overline{A}_2$
20	B_2	$\overline{B}_2$
19	A_3	$\overline{A}_3$
18	B_3	$\overline{B}_3$
9	F_0	$\overline{F}_0$
10	F_1	$\overline{F}_1$
11	F_2	$\overline{F}_2$
13	F_3	$\overline{F}_3$
7	$\overline{C}_n$	C_n
16	$\overline{C}_{n+4}$	C_{n+4}
15	X	$\overline{P}$
17	Y	$\overline{G}$

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

These devices can also be utilized as comparators. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

Input C_n	Output C_{n+4}	(Figure 1) Active-high Data	(Figure 2) Active-low Data
H	H	$A \leqslant B$	$A \geqslant B$
H	L	$A > B$	$A < B$
L	H	$A < B$	$A > B$
L	L	$A \geqslant B$	$A \leqslant B$

Continued....

100000084 100000169 100000306

Continued

Figure 1

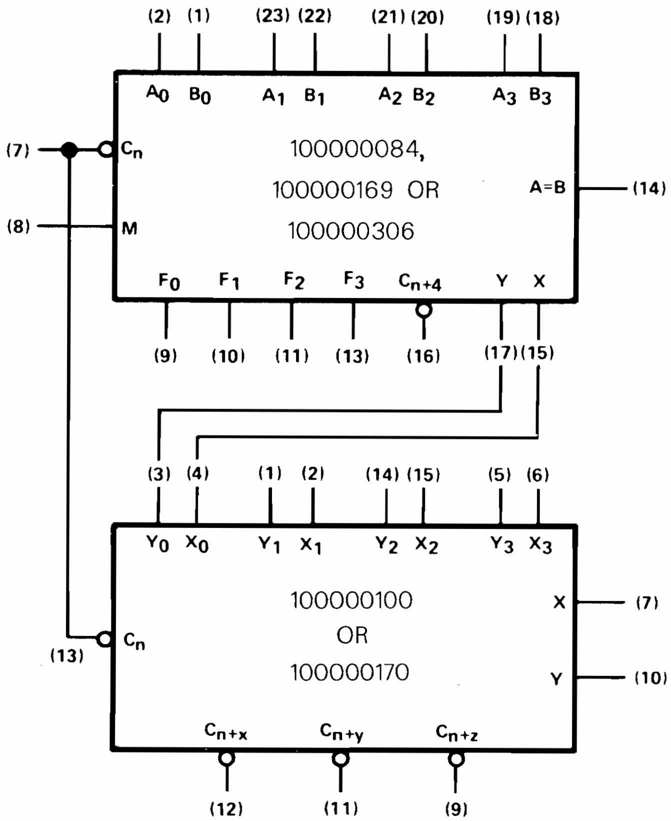
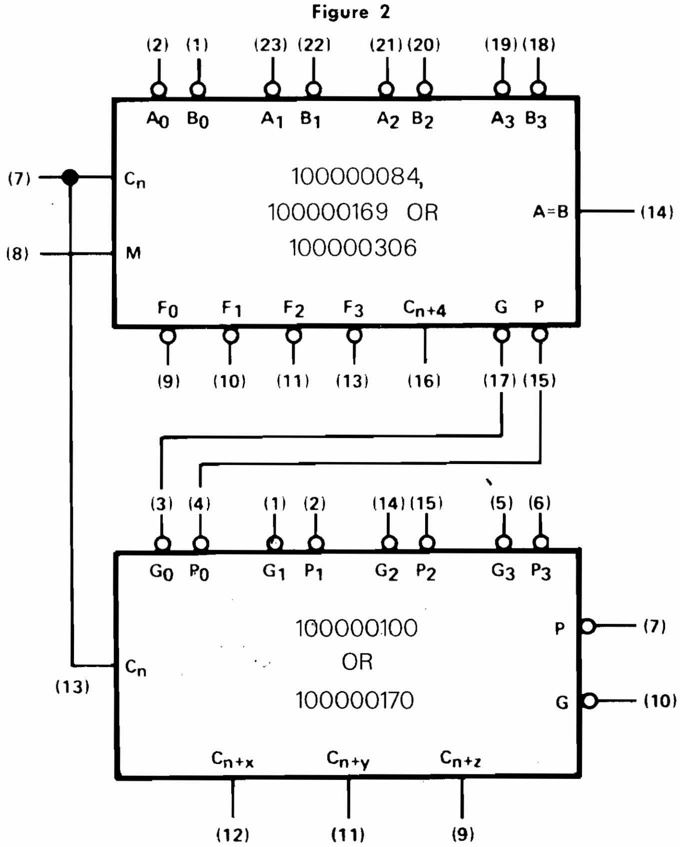


Figure 2



These circuits have been designed to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR and OR functions.

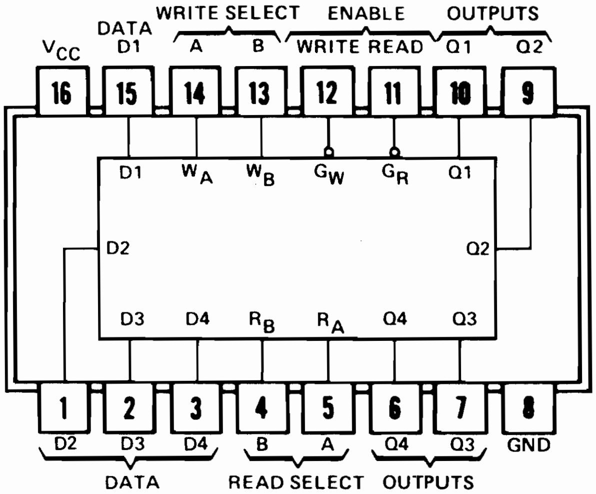
ALU Signal Designations

These devices can be used with the signal designations of either Figure 1 or Figure 2. The logic functions and arithmetic operations obtained with the signal designations of Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

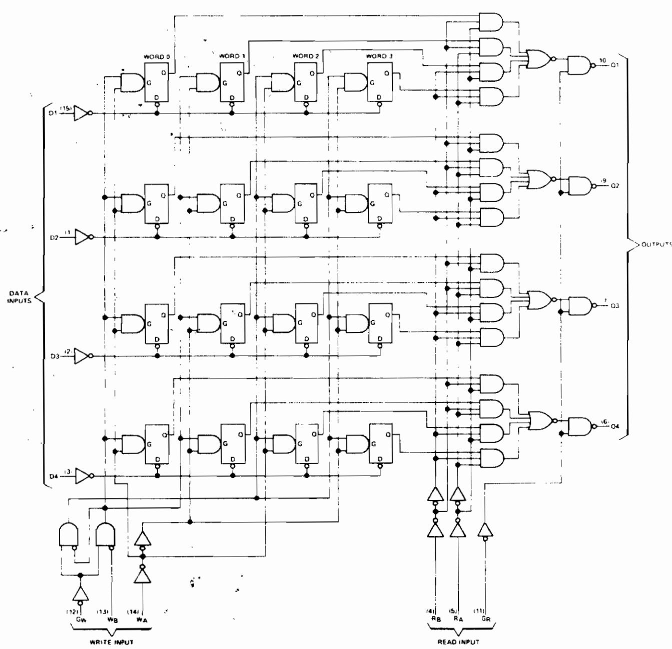
Note: The 100000169 is a Schottky device.

100000085

Pin Configuration



Logic Diagram



4-By-4 Register File

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

The 100000085 16-bit TTL register file is organized as 4 words of 4 bits each. Separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data; this permits simultaneous writing into one location and reading from another word location. The register file has a nondestructive readout in that data is not lost when addressed.

Four data inputs are available which are used to supply 4-bit words to be stored. Location of the word is determined by the write address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form; that is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read enable input, G_R, is high, the data outputs are inhibited and remain high.

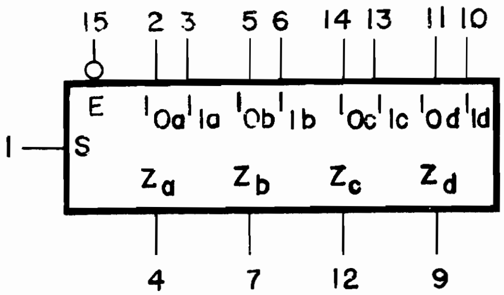
The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of registers may be paralleled to provide n-bit word length.

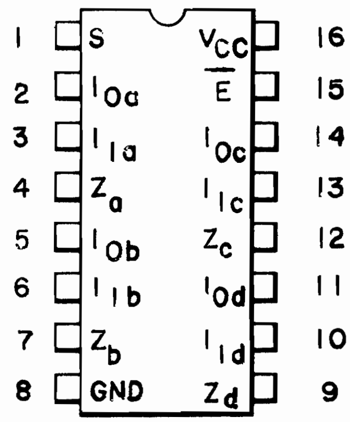
100000086

Quad Two-Input Multiplexer

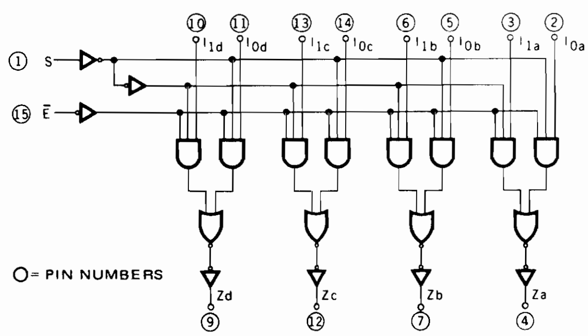
Logic Symbol



Logic Diagram



Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

S	Common Selected Input
$\overline{E}$	Enable (Active LOW)Inputs
$I_{0a}, I_{1a}, I_{0b}, I_{1b}$, $I_{0c}, I_{1c}, I_{0d}, I_{1d}$	Multiplexer Inputs
Z_a, Z_b, Z_c, Z_d	Multiplexer Output

Truth Table

Enable	Select Input	Inputs		Output
$\overline{E}$	S	I_{0X}	I_{1X}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Logic Level

The 100000086 Quad Two-Input Multiplexer consists of four multiplexing circuits with common select and enable logic; each circuit contains two inputs and one output. The Enable input ($\overline{E}$) is active LOW. When not activated, all outputs (Z) are LOW regardless of other inputs.

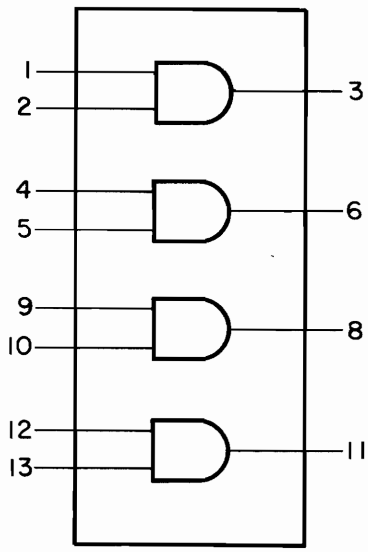
The multiplexer is the logical implementation of a four-pole, two-position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs follow:

$$Z_a = E \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$Z_b = E \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = E \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$Z_d = E \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

100000089

Quad 2-Input AND Gate

Pin Configuration



Logic Diagram/Pin Designations

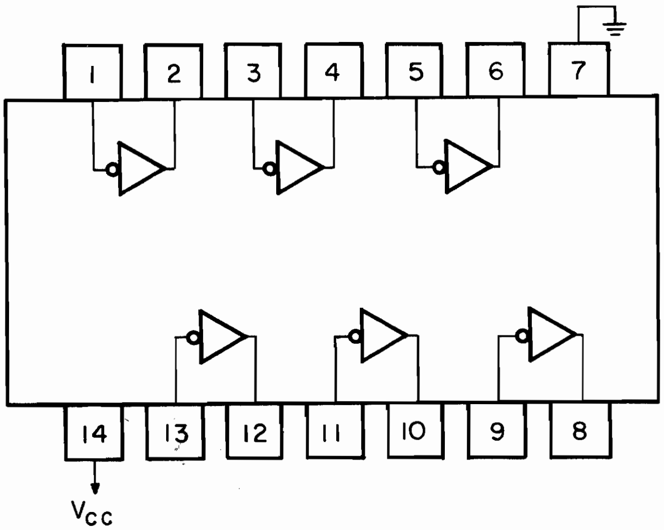
V_{CC} = Pin 14

Gnd = Pin 7

3 = 1 · 2

100000090

Pin Configuration



6-Input Hex Inverter

Logic Diagram/Pin Designations

V_{CC} = Pin 14

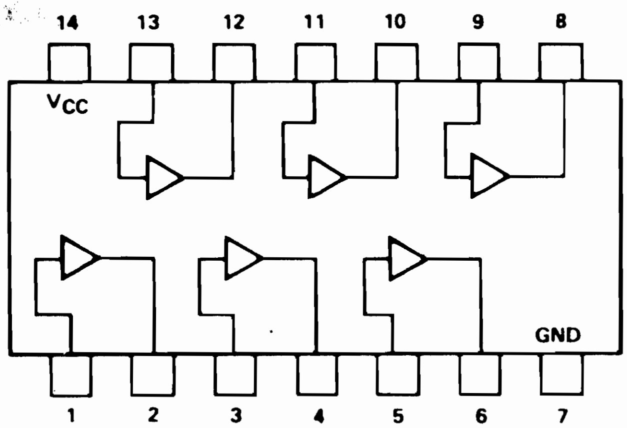
Gnd = Pin 7

Positive logic: $Y = \overline{AB}$

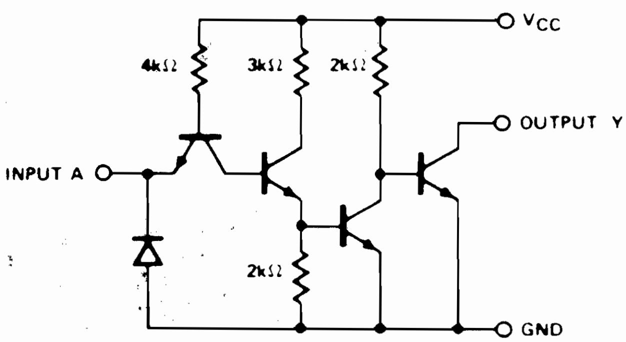
100000091

Hex Buffer/Driver with Open Collector High Voltage Outputs

Pin Configuration



Schematic (Each Buffer/Driver)



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

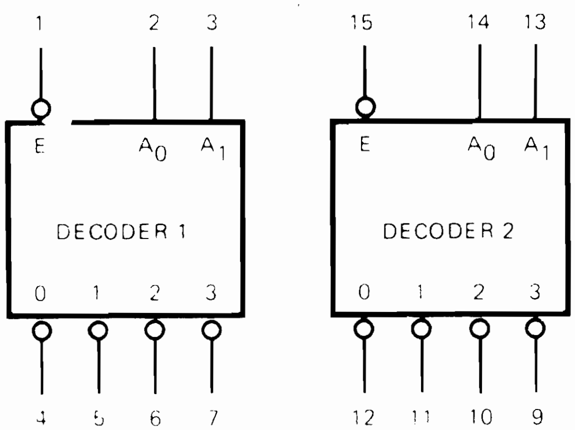
Positive logic: Y = A

The 100000091 has standard TTL inputs with non-inverted high voltage, high current open collector outputs for interface with MOS, lamps or relays.

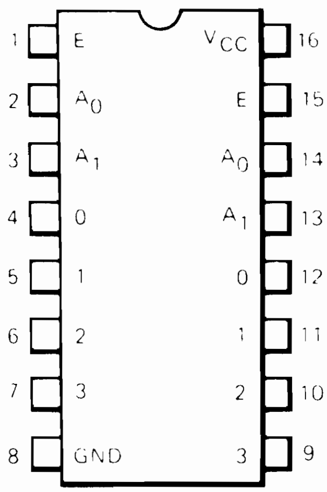
100000092

Dual One-of-Four Decoder

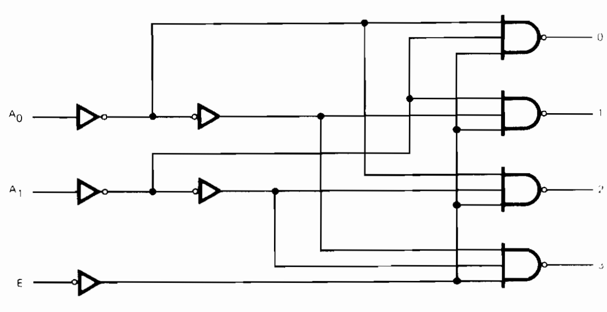
Logic Symbol



Pin Configuration



Logic Diagram



Note: Only one Decoder shown.

Logic Diagram/Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Pin Names

Decoder 1 and 2

$\overline{E}$ .... Enable (Active LOW) Input
A_0, A_1 .... Address Inputs
$\overline{0}, \overline{1}, \overline{2}, \overline{3}$ .... (Active LOW) Outputs

Truth Table
Decoder 1 & 2

$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

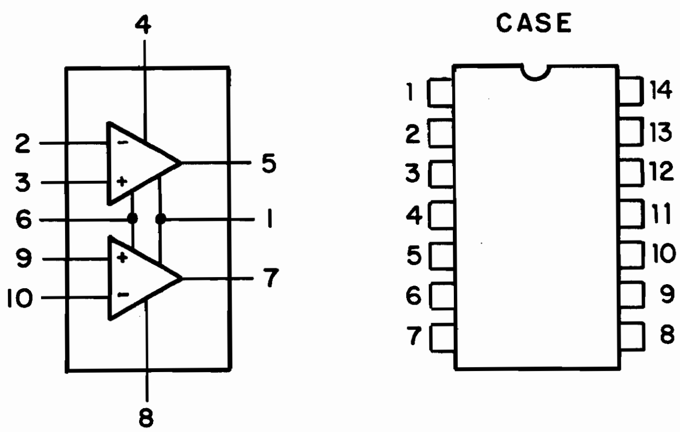
The 100000092 consists of two independent multipurpose decoders, each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

The active LOW outputs facilitate memory addressing for units such as the 100000211 associative memory.

100000093

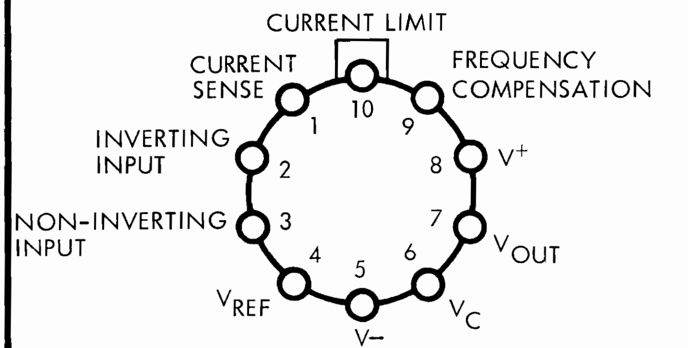
Monolithic Dual Operational Amplifier

Pin Configuration



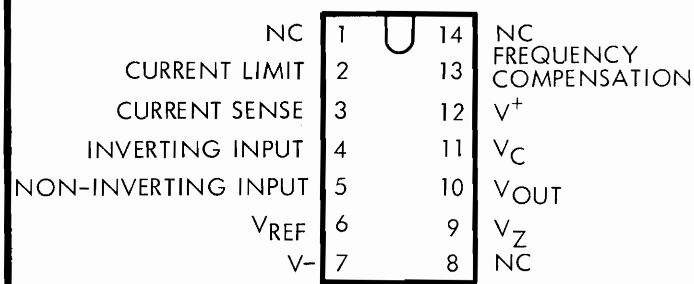
100000026 10000094 100000318

Pin Configurations



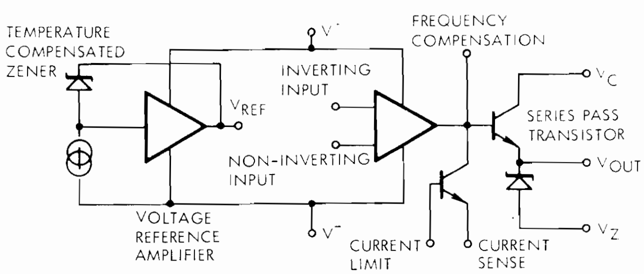
Note: pin 5 is connected to case

100000026



100000094

Equivalent Circuit

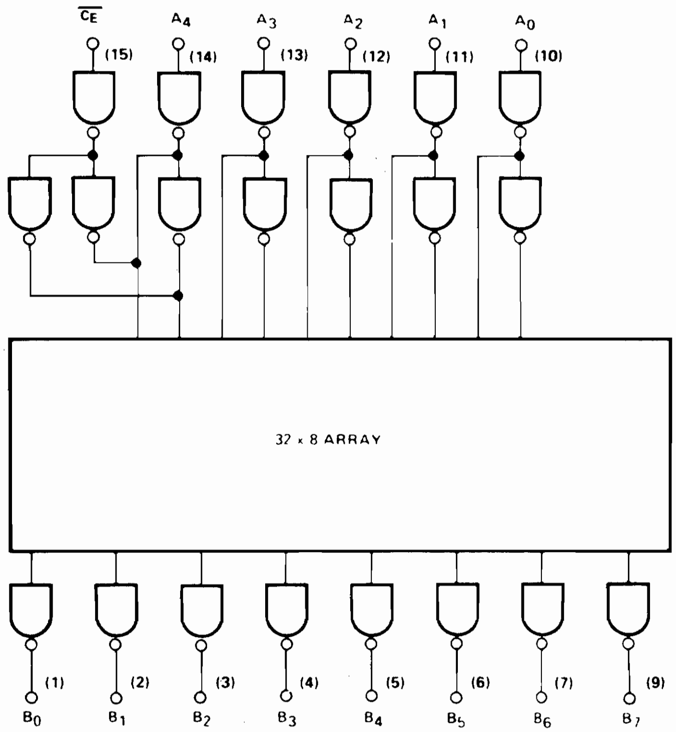


Precision Voltage Regulator

The 100000026(Can) and 100000094, 100000318(DIP) are monolithic voltage regulators, consisting of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150mA are required. Provisions are made for adjustable current limiting and remote shutdown.

REV. 03

Logic Diagram



256-Bit Bipolar ROM

Logic Diagram/Pin Designations

V_{CC} = Pin 16

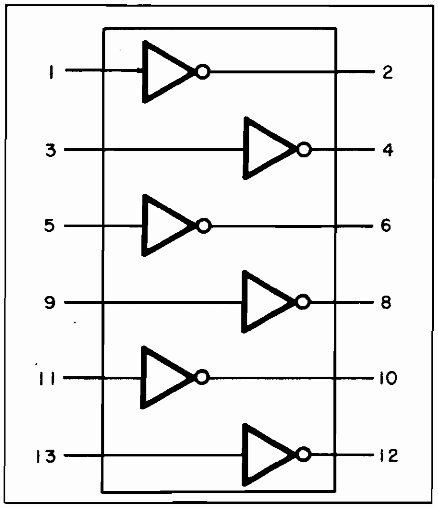
Gnd = Pin 8

These TTL 256-bit read only memories are organized as 32 words with 8 bits per word. The words are selected by five binary address lines with full word decoding incorporated on the chip. A Chip Enable input is provided for additional decoding flexibility, which will cause all eight outputs to go to the high state when the Chip Enable input is taken high.

The 100000095 and 100000096 are fully TTL or DTL compatible. The outputs are uncommitted collectors, which allows wired-AND operation with the outputs of other TTL or DTL devices.

100000098

Pin Configuration



Hex Inverter

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

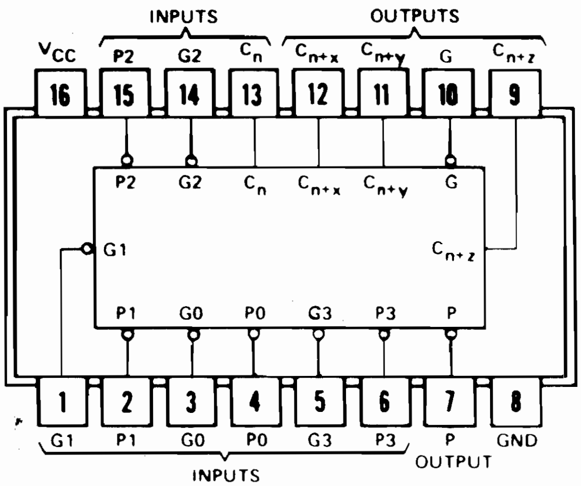
Truth Table

Any Input Low = High Out
Any Input High = Low Out

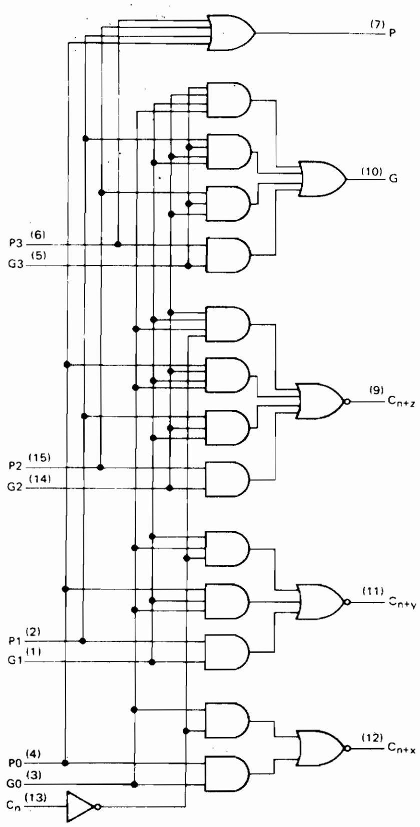
100000100 100000170

Look-Ahead Carry Generators

Pin Configuration



Logic Diagram



Pin Designations

Designation	Pin Nos.	Function
G0, G1, G2, G3	3, 1, 14, 5	Active-Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active-Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active-Low Carry Generate Output
P	7	Active-Low Carry Propagate Output
V_{CC}	16	Supply Voltage
Gnd	8	Ground

Positive Logic:

$$C_{n+x} = \overline{G}_0 + \overline{P}_0 C_n$$
$$C_{n+y} = \overline{G}_1 + \overline{P}_1\overline{G}_0 + \overline{P}_1\overline{P}_0 C_n$$
$$C_{n+z} = \overline{G}_2 + \overline{P}_2\overline{G}_1 + \overline{P}_2\overline{P}_1\overline{G}_0 + \overline{P}_2\overline{P}_1\overline{P}_0 C_n$$
$$\overline{G} = \overline{G}_3(\overline{P}_3+\overline{G}_2)(\overline{P}_3+\overline{P}_2+\overline{G}_1)(\overline{P}_3+\overline{P}_2+\overline{P}_1+\overline{G}_0)$$
$$\overline{P} = \overline{P}_3\overline{P}_2\overline{P}_1\overline{P}_0$$

These devices are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry and propagate-carry functions are provided as enumerated in the pin designation table above.

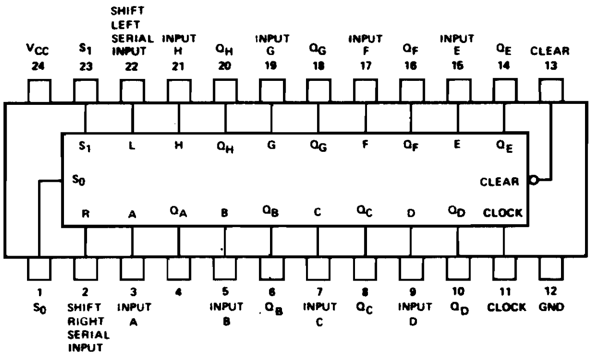
When used in conjunction with arithmetic logic units, 100000084 or 100000169, these generators provide high-speed carry look-ahead capability for any word length.

Carry input and output of the 100000084 or 100000169 are in their true form and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU.

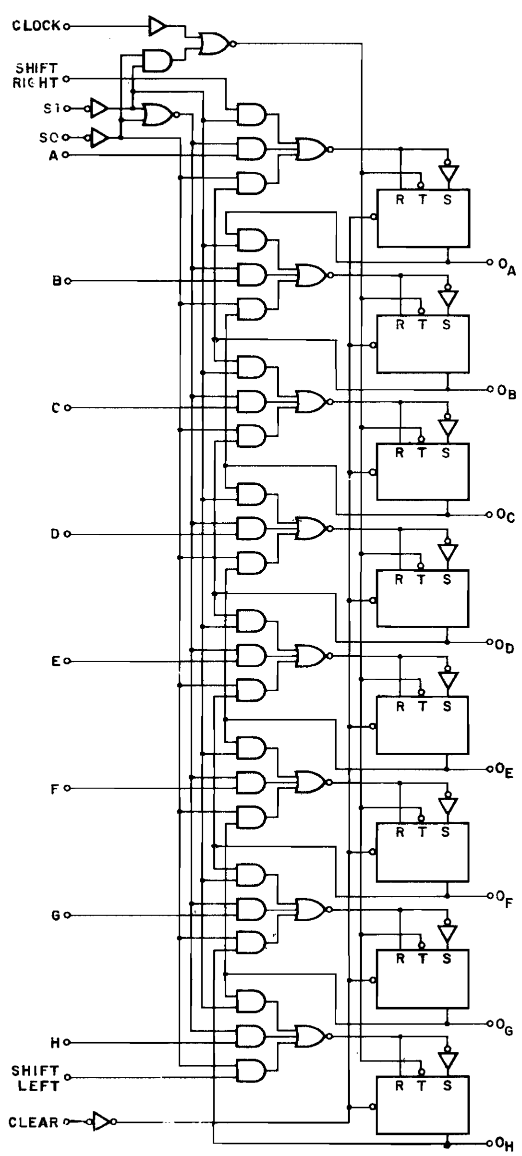
Note: The 100000170 is a Schottky device.

100000101

Pin Configuration



Logic Diagram



8-Bit Shift Register

Pin Designations

V_{CC} = Pin 24

Gnd = Pin 12

Truth Table

Operation of Mode Control		
Inputs		Mode
S_1	S_0	
L	L	Inhibit Clock
H	L	Shift Left
L	H	Shift Right
H	H	Parallel Load

This 8-bit shift register contains 87 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load

Shift Right (in the direction Q_A toward Q_H)

Shift Left (in the direction Q_H toward Q_A)

Inhibit Clock (do nothing)

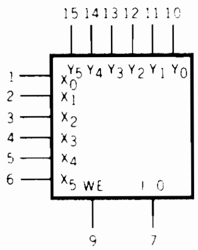
Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

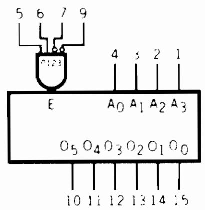
Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

100000102 100000103

Logic Symbols

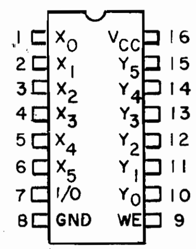


100000102

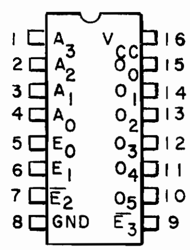


100000103

Connection Diagrams

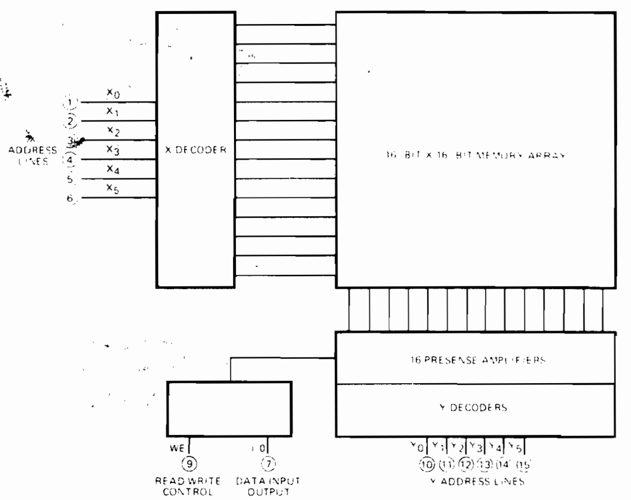


100000102



100000103

Logic Diagram



○ = PIN NUMBERS

256-Bit Read/Write Memory & Decoder/Driver

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Truth Table

Binary Input To 100000103				3 of 6 Code Output of 100000103 Input to 100000102 (L = O or X or Y)						100000102 Internal X or Y Address
A_3	A_2	A_1	A_0	L_0	L_1	L_2	L_3	L_4	L_5	Row or Column
L	L	L	L	H	H	L	L	L	H	0
L	L	L	H	H	L	H	L	L	H	1
L	L	H	L	H	L	L	H	L	H	2
L	L	H	H	H	L	L	L	H	H	3
L	H	L	L	H	H	H	L	L	L	4
L	H	L	H	H	L	H	L	H	L	5
L	H	H	L	H	H	L	H	L	L	6
L	H	H	H	H	L	L	H	H	L	7
H	L	L	L	L	H	L	H	L	H	8
H	L	L	H	L	H	H	L	L	H	9
H	L	H	L	L	L	L	H	H	H	10
H	L	H	H	L	L	H	L	H	H	11
H	H	L	L	L	H	H	H	L	L	12
H	H	L	H	L	H	H	L	H	L	13
H	H	H	L	L	H	L	H	H	L	14
H	H	H	H	L	L	H	H	H	L	15

Note: Enables on 100000103 must be LLHH. Any other state on the enable inputs causes the Decoder/Driver outputs to go LOW, and addresses no internal row or column in the 100000102 memory matrix.

The 100000102 256-Bit Read/Write Memory and the 100000103 Decoder/Driver are components for use in high speed memory systems.

The 100000102 contains 256 bipolar storage cells arranged in a 16 by 16 format. Any one of the 256 cells may be accessed by supplying an address code on the X address inputs and the Y address inputs. Internal decoders decode the X and Y addresses into one of 16 rows and one of 16 columns in the matrix of storage cells. Data may be written into or read out from the cell lying at the intersection of the selected row and column.

The X and Y addresses supplied to the memory are partially decoded in a "3 of 6" code. Of the six X address lines and the six Y address lines there are always three lines HIGH and three

Continued ....

lines LOW. There are 20 such combinations, 16 are decoded by the internal row and column decoders. The four unused combinations of 3 of 6 will not select any row or column. If there are more than three lines HIGH in either the X or Y address, then multiple row or column selection will occur. The sixteen 3 of 6 codes used by the 100000102 memory are generated by the 100000103 decoder/driver.

Data enters and leaves the memory on a single input/output (I/O) line (pin 7). The I/O line is an open collector output, so many 100000102 I/O lines can be connected together in a wired-OR configuration. Input data must be applied to the I/O lines through an open collector gate. Each I/O line requires a pull-up resistor to V_{CC}. The magnitude of the pull-up resistor is determined by the number of memory I/O lines tied together. The I/O of the memory which is not addressed will be HIGH.

Read/Write selection is determined by the state of pin 9, the active HIGH write enable. When WE is HIGH, the data on the I/O line will be written into the selected address in the 100000102. When the Write Enable line is LOW, data will be read out of the addressed location.

The 100000103 is a partial decoder and driver for the 100000102. It accepts a 4-bit binary code on the address inputs (A_0-A_3) and produces a 3 of 6 code on the six output pins (O_0-O_5). The decoder also features four separate enables, two active HIGH and two active LOW. All four enables must be active before the decoder will produce a 3 of 6 code. Since two of the enables are HIGH and two are LOW, it is possible to route two binary coded lines to four different 100000103's to get two additional bits of decoding with no extra packages.

Ordinarily in memory systems, 100000102 memory devices will be arranged in a matrix of rows and columns. Each column will store a particular bit and each row of 100000102's will be 256 words. A 100000103 driver will be used for each row and each column in the matrix. One 100000103 can drive up to 32 100000102 X or Y address lines. The usual driving scheme is to connect the four LSB's of address to each of the column decoders. The next four bits of address are connected to each of the row decoders. Additional address bits are decoded to the chip selects on the row decoders. Each column decoder drives the Y address lines on up to 32 100000102's in a column. Each row decoder drives the address lines on up to 32 100000102's in a row.

The Three of Six Code

The "3 of 6" code used in the 100000102 and produced by the 100000103 is a trade-off between chip complexity and pin count. The simplest 256-bit memory chip would be a 16 by 16 matrix of storage cells, with all 16 rows and 16 column select lines brought off chip. The lowest pin count for a 256-bit memory chip would be achieved by fully decoded X and Y select lines, reducing the 32 lines of the simple scheme to only 8 lines. However, full binary decoding of the X and Y lines on chip significantly increases the complexity of the memory chip. The 100000102 and 100000103 are designed to gain the good features of both alternatives. The 16 X and Y lines are decoded into 6 lines each, allowing the memory to fit into a 16-lead package and still keeping the memory chip fairly simple, since the 3 of 6 code does not require a complex decoder. The truth table shows the conversion of 4-bit binary to 3 of 6 code by the 100000103, and also the internal column or row selected by the 3 of 6 to 1 of 16 decoder inside the memory.

Code Conversion Equations

$$O_0 = \overline{A_3}$$

$$O_1 = \overline{(A_1 + A_0)\ (\overline{A_3} + A_1)\ (\overline{A_2} + A_0)}$$

$$O_2 = \overline{(A_1 + \overline{A_0})\ (\overline{A_3} + \overline{A_0})\ (A_2 + \overline{A_1})}$$

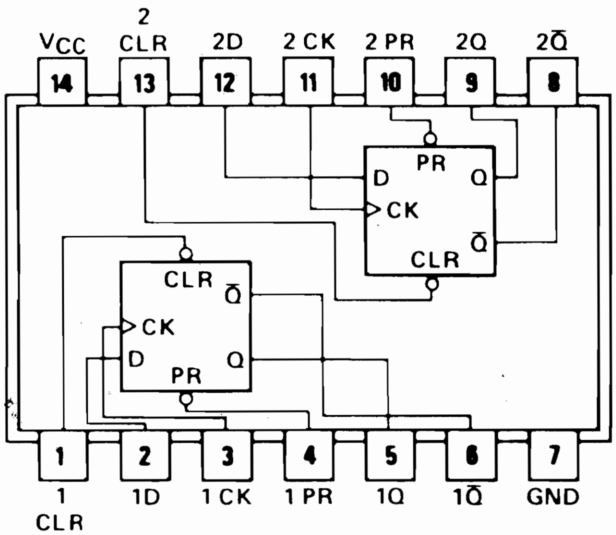
$$O_3 = \overline{(\overline{A_1} + A_0)\ (\overline{A_3} + A_0)\ (\overline{A_2} + \overline{A_1})}$$

$$O_4 = \overline{(\overline{A_1} + \overline{A_0})\ (\overline{A_3} + \overline{A_1})\ (\overline{A_2} + \overline{A_0})}$$

$$O_5 = \overline{A_2}$$

100000104

Pin Configuration



Dual D-Type Positive-Edge-Triggered Flip-Flops With Preset and Clear

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Function Table

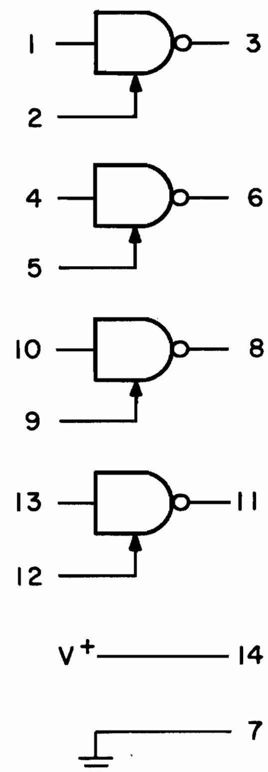
Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

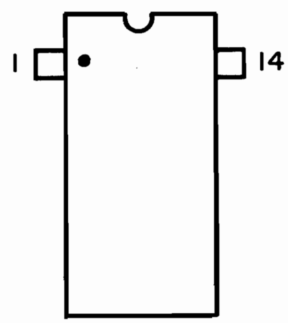
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

100000105

Quad Line Receivers

Logic Diagram

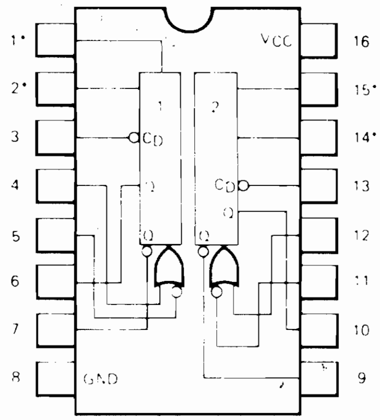




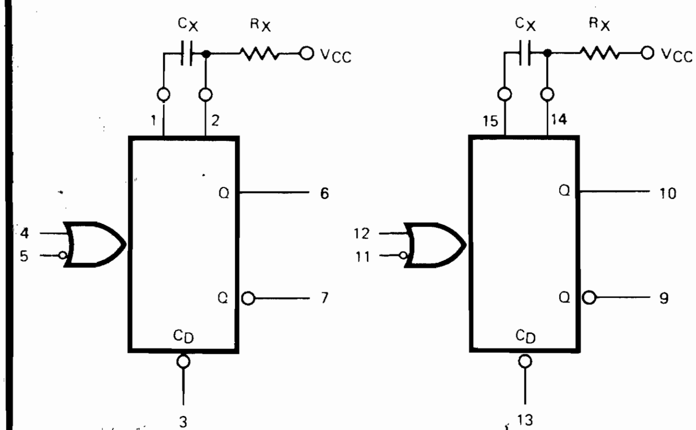
100000106 100000321

Dual Retriggerable Resettable Monostable Multivibrator

Pin Configuration



Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Triggering Truth Table

Pin Numbers			
5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

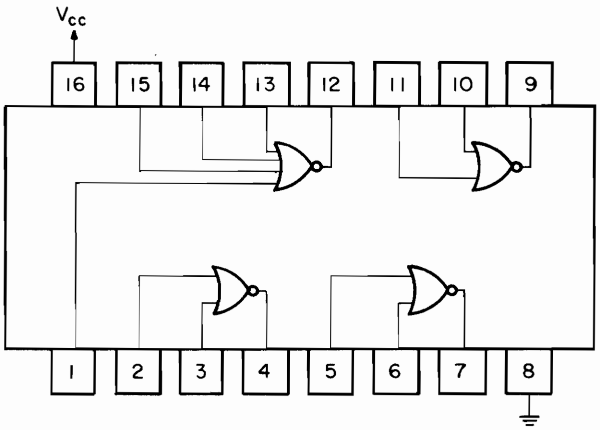
H = HIGH Voltage Level $\geqslant V_{IH}$
L = LOW Voltage Level $\leqslant V_{IL}$
X = Don't Care
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

The Dual Retriggerable, Resettable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components.

This device has two inputs per function, one active LOW and one active HIGH. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the device and result in a continuous true output. The output pulse may be terminated at any time by connecting the reset pin to a logic level LOW. Retriggering may be inhibited by tying $\overline{Q}$ output to an active level LOW input or the Q output to the active level HIGH input.

100000107

Pin Configuration



Quad NOR Gate

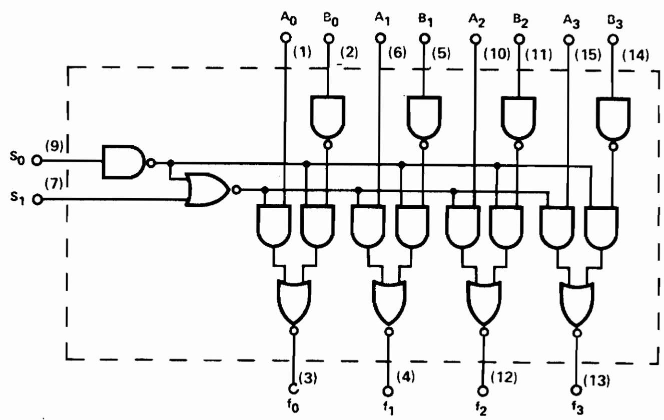
Logic Diagram/Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

The 100000107 consists of three 2-input and one 4-input NOR gates. The NOR gate produces a Low output if any of the inputs are High.

100000057 100000108

Logic Diagram



2-Input, 4-Bit Digital Multiplexer

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

Select Lines		Outputs
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	1

The 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing TTL circuit structures. The 100000108 features a bare-collector output to allow expansion with other devices.

The multiplexer is able to choose from two different input sources, each containing 4 bits: A = (A_0, A_1, A_2, A_3); B = (B_0, B_1, B_2, B_3). The selection is controlled by the input S_0, while the second control input, S_1, is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with added elements to perform Addition/ Subtraction. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

100000109 100000125 100000111 100000382

Buffer Registers

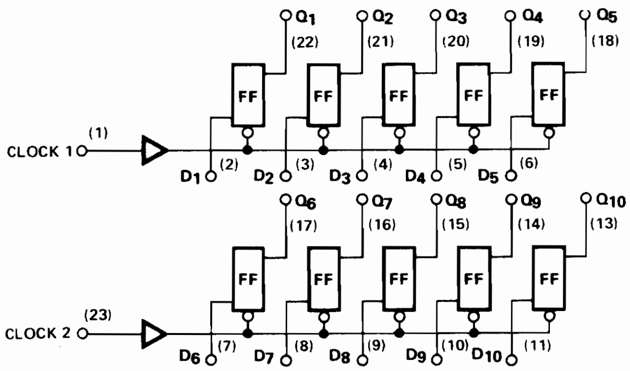
Logic Diagram/Pin Designations

V_{CC} = Pin 24

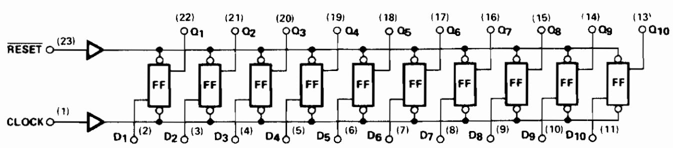
Gnd = Pin 12

Logic Diagrams

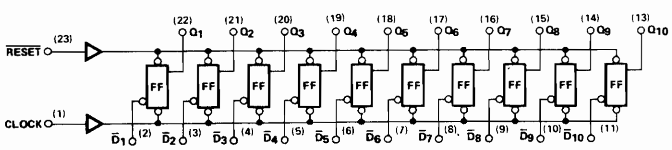
100000111, 100000382



100000109



100000125



Truth Tables

Dual 5-Bit Buffer Registers Nos. 100000111 and 100000382

D_n	Q_{n+1}
1	1
0	0

10-Bit Buffer Register No. 100000109

D_n	$\overline{RESET}$	Q_{n+1}
1	1	1
0	1	0

10-Bit Buffer Register-Inverted Inputs No. 100000125

D_n	$\overline{RESET}$	Q_{n+1}
0	1	1
1	1	0

Notes:

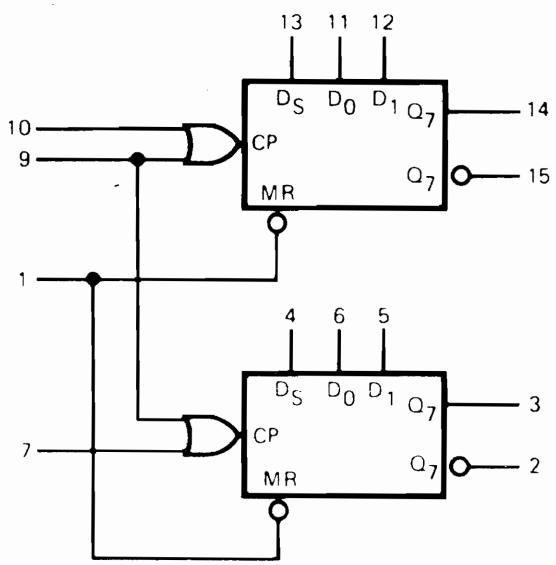
$\overline{RESET} = 0 \Rightarrow Q = 0$ (overrides clock).
n is time prior to clock.
n+1 is time following clock.

These buffer registers are arrays of ten clocked "D" flip-flops. The flip-flops are arranged as a dual 5 array (100000111 & 100000382) and single 10 arrays with reset (100000109 and 100000125).

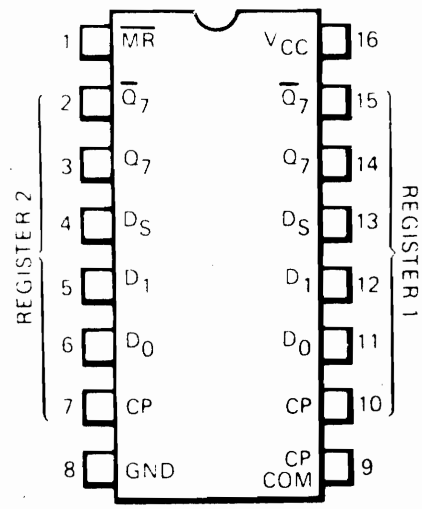
The 100000111, 100000382 and 100000109 have true "D" inputs. The logic state presented at these "D" inputs will appear at the Q outputs after a negative transition of the clock. The 100000125 has complementing "D" inputs ("$\overline{D}$"). The logic state presented at these "$\overline{D}$" inputs will invert and appear at the Q outputs after a negative-going transition of the clock. The complementing input ("$\overline{D}$") permits the use of standard AND-OR-INVERT gates to achieve the AND-OR function without additional gate delays.

100000112

Logic Symbol



Pin Configuration



Dual 8-Bit Shift Register

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

D_S .... Data Select Input
D_0, D_1 .... Data Inputs
CP .... Clock (Active HIGH) Going Edge Input
Common (Pin 9)
Separate (Pins 7 and 10)
$\overline{MR}$ .... Master Reset (Active LOW) Input
Q_7 .... Last Stage Output
$\overline{Q_7}$ .... Complementary Output

Truth Table
Shift Selection

D_S	D_0	D_1	Q_7 (t_{n+8})
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

n+8 = Indicates state after eight clock pulse.
L = LOW voltage level
H = HIGH voltage level
X = Either HIGH or LOW voltage level

This device is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers that will shift at greater than 20 MHz rates. The multi-functional capability of this device is provided by several features: 1) Additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources. 2) The clock of each register may be provided separately or together. 3) Both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW to HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later

Continued....

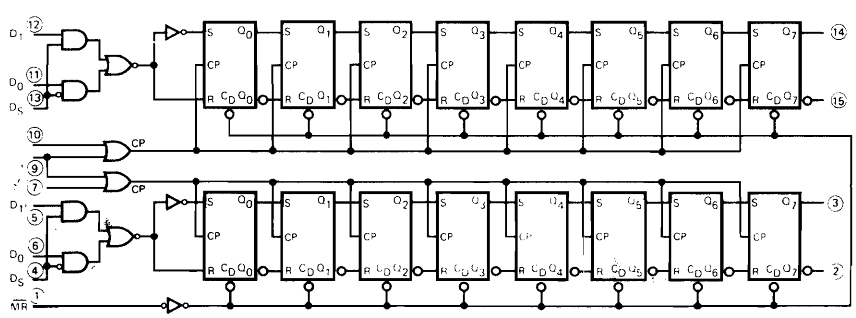
10000112
Continued

change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH to LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register has a two input multiplexer in front of the serial data input. The two data inputs, D_0 and D_1, are controlled by the data select input (D_S) following the Boolean expression:

$$\text{Serial data in: } S_D = \overline{D}_S D_0 + D_S D_1$$

An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all sixteen stages independently of any other input signal.

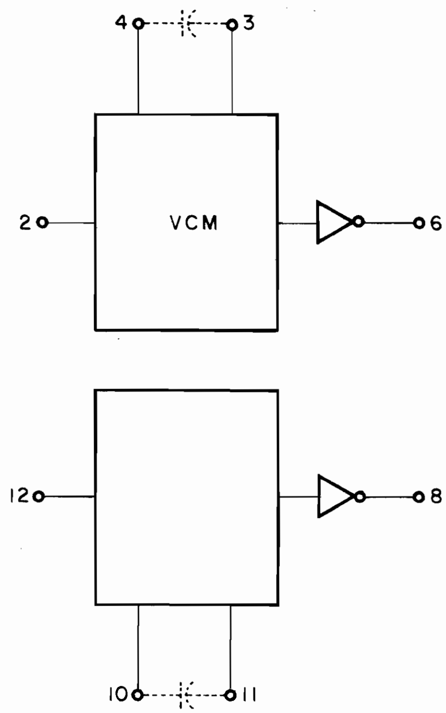
Logic Diagram



○ = Pin Numbers

100000114

Functional Block Diagram



Dual Voltage Controlled Multivibrator

Pin Designations

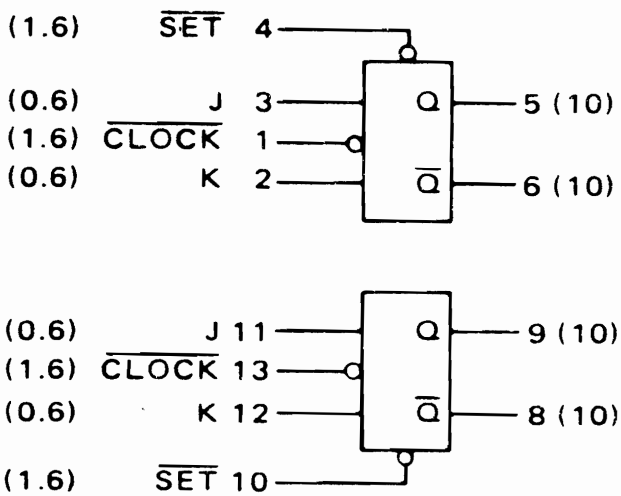
V_{cc}: VCM = 1, 3
Output Buffer = 14

Gnd: VCM = 5, 9
Output Buffer = 7

External capacitor for frequency range determination.

100000115

Logic Diagram



Dual J-K Flip-Flop

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

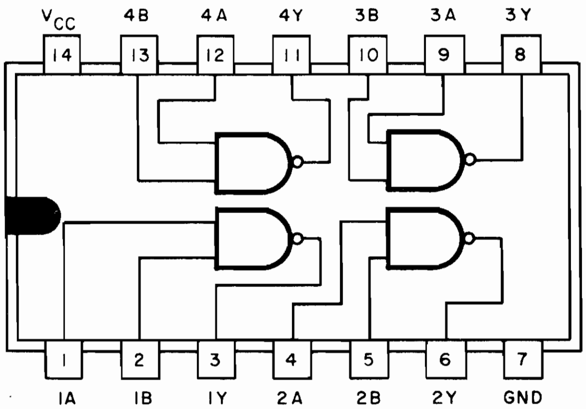
Truth Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

100000116

Quadruple 2-Input Positive-NAND Buffer

Pin Configuration



Logic Diagram/Pin Designations

V_{CC} = Pin 14

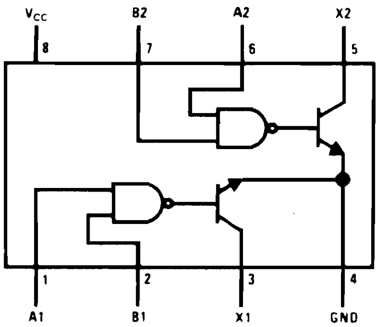
Gnd = Pin 7

Positive logic: $Y = \overline{AB}$

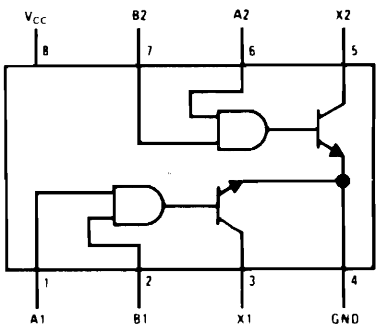
100000228 100000247 100000238 100000154 100000117

Dual Peripheral Drivers

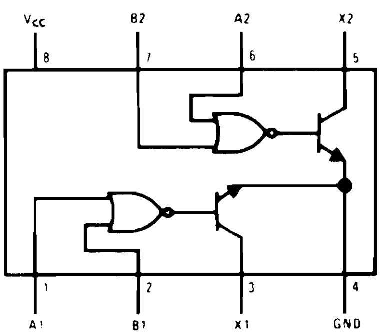
Pin Configurations



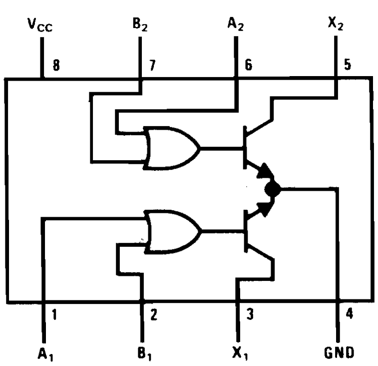
100000247/100000238



100000154



100000117



100000228

V_{CC} = Pin 8
Gnd = Pin 4

Truth Tables

100000247 and 100000238

Positive logic: AB=X

A	B	Output X*
0	0	0
1	0	0
0	1	0
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000154

Positive logic: $\overline{AB}$=X

A	B	Output X*
0	0	1
1	0	1
0	1	1
1	1	0

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000117

Positive logic: A + B = X

A	B	Output X*
0	0	0
1	0	1
0	1	1
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

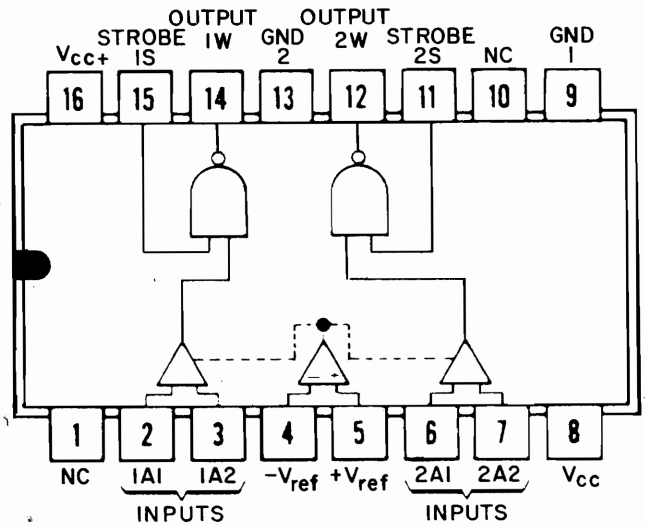
100000228
Truth Table

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible.

100000118 100000229
100000298 100000299

Pin Configuration



Dual Sense Amplifiers

Logic Diagram/Pin Designations

V_{CC+} = Pin 16
V_{CC} = Pin 8
Gnd 1 = Pin 9
Gnd 2 = Pin 13
NC = No internal connection

Positive logic: $W = \overline{AS}$

Truth Table

Inputs		Output
A	S	W
H	H	L
L	X	H
X	L	H

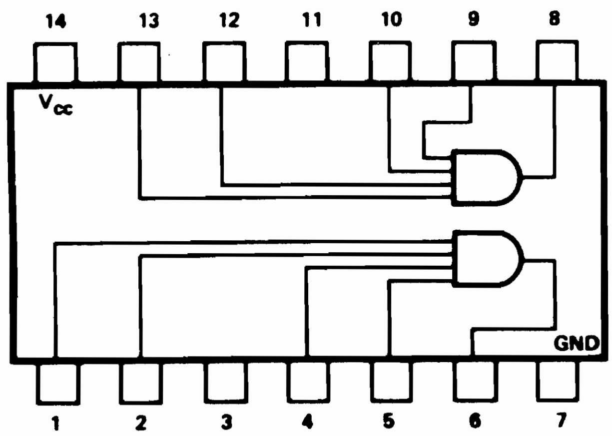
Definition of logic levels:

Input	H	L	X
A*	$V_{ID} \geqslant V_{Tmax}$	$V_{ID} \leqslant V_{Tmin}$	Irrelevant
S	$V_I \geqslant V_{IHmin}$	$V_I < V_{ILmax}$	Irrelevant

* A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

100000119

Pin Configuration



Dual 4-Input Positive-AND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

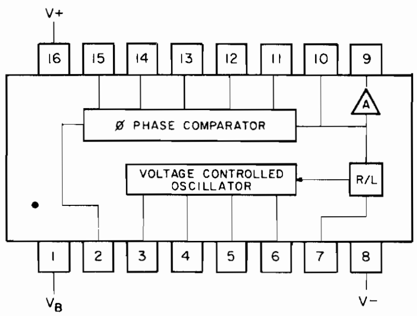
Gnd = Pin 7

Positive logic: Y = ABCD

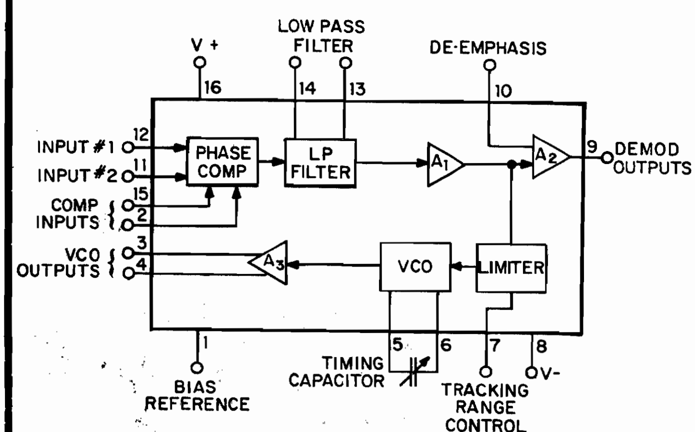
100000120

Phase Locked Loop

Pin Configuration



Block Diagram



Pin Designations

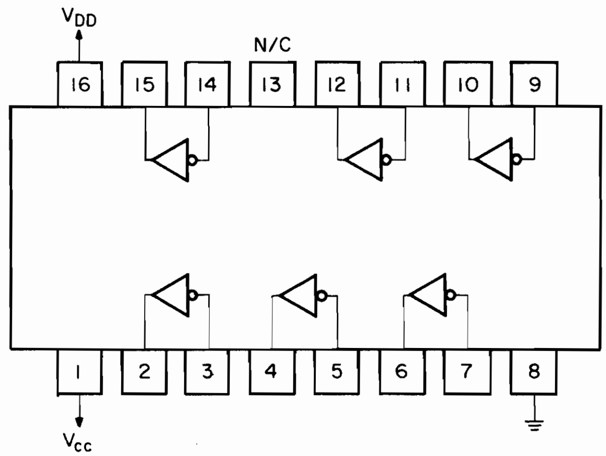
1. Bias Reference Voltage
2. Phase Comparator Input #1
3. VCO Output #1
4. VCO Output #2
5. VCO Timing Capacitor
6. VCO Timing Capacitor
7. Range Control
8. Negative Power Supply (Ground)
9. Demodulated FM Output (Open Emitter)
10. De-emphasis (Auto Bandshaping)
11. RF Input #1
12. RF Input #2
13. Low Pass Loop Filter
14. Low Pass Loop Filter
15. Phase Comparator Input #2
16. Positive Power Supply

The 100000120 Phase Locked Loop is a monolithic signal conditioner and demodulator system, comprising a VCO, phase comparator, amplifier and low pass filter.

The center frequency of the Phase Locked Loop is determined by the free running frequency of the VCO. This VCO frequency is set by an external capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by two capacitors and two resistors at the phase comparator output. This Phase Locked Loop has two sets of differential inputs, one for the FM/RF input and one for the phase comparator local oscillator input. Both sets of inputs can be used in either a differential or single-ended mode. The FM/RF inputs to the comparator are self-biased. An internally regulated voltage source is provided to bias the phase comparator local oscillator inputs. The VCO output, at high level and in differential form, is available for driving logic circuits.

100000121

Pin Configuration



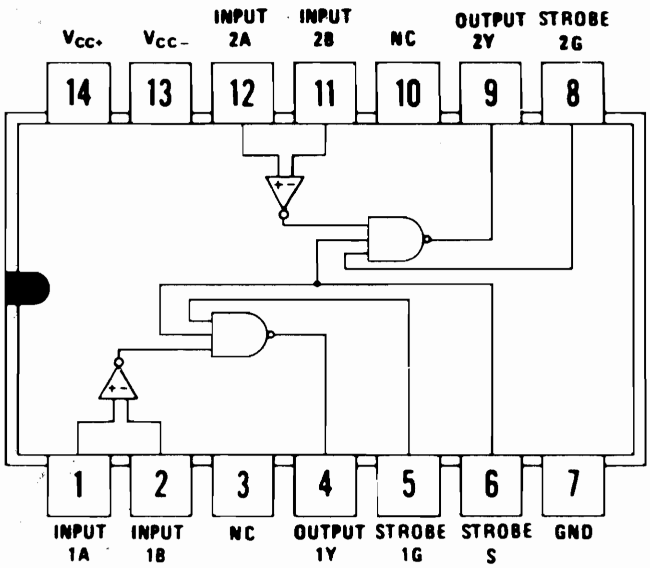
CMOS Hex Inverter

Logic Diagram/Pin Designations

V_{CC} = Pin 1
V_{DD} = Pin 16
Gnd = Pin 8

100000122

Pin Configuration



Dual Line Receiver

Logic Diagram/Pin Designations

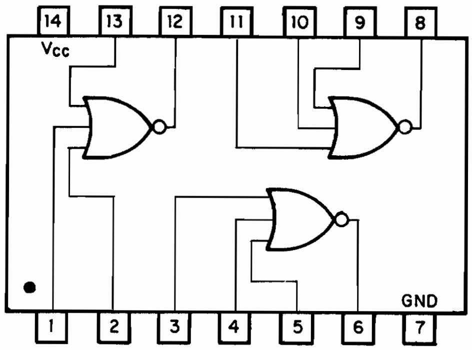
V_{CC+} = Pin 14
V_{CC-} = Pin 13
Gnd = Pin 7
NC = No internal connection

Truth Table

Differential Inputs A-B	Strobes G	Strobes S	Output Y
$V_{ID} \geqslant 25mV$	L or H	L or H	H
$-25mV < V_{ID} < 25mV$	L or H	L	H
	L	L or H	H
	H	H	Indeter-minate
$V_{ID} \leqslant -25mV$	L or H	L	H
	L	L or H	H
	H	H	L

100000123

Pin Configuration



Triple 3-Input NOR Gate

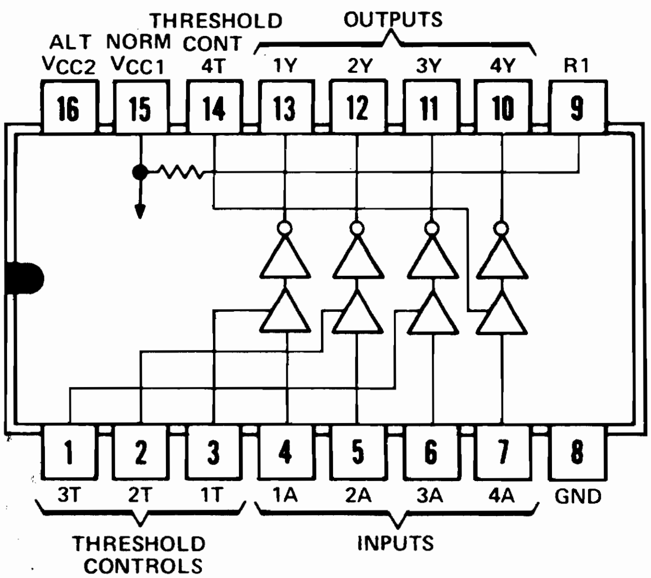
Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

100000124

Pin Configuration



Quadruple Line Receiver

Logic Diagram/Pin Designations

V_{CC1} = Pin 15

V_{CC2} = Pin 16

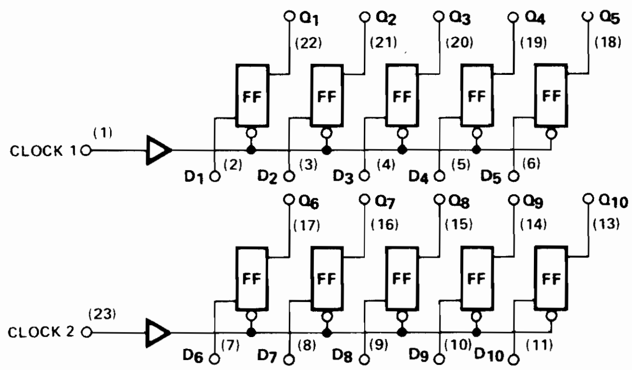
Gnd = Pin 8

Logic: $Y = \overline{A}$

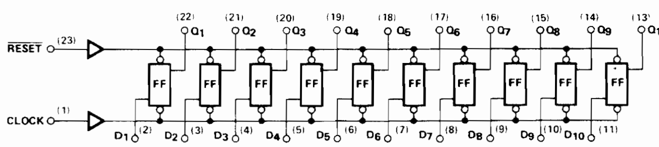
100000109 100000111 100000125 100000382

Logic Diagrams

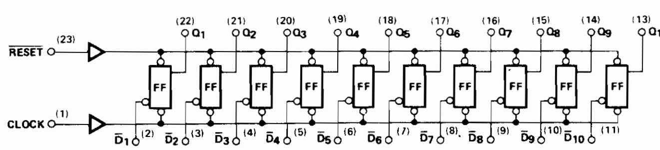
100000111, 100000382



100000109



100000125



Buffer Registers

Logic Diagram/Pin Designations

V_{CC} = Pin 24

Gnd = Pin 12

Truth Tables

Dual 5-Bit Buffer Registers Nos. 100000111 and 100000382

D_n	Q_{n+1}
1	1
0	0

10-Bit Buffer Register No. 100000109

D_n	$\overline{RESET}$	Q_{n+1}
1	1	1
0	1	0

10-Bit Buffer Register-Inverted Inputs No. 100000125

D_n	$\overline{RESET}$	Q_{n+1}
0	1	1
1	1	0

Notes:

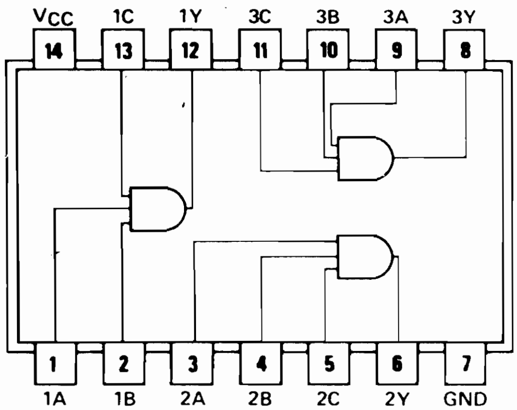
$\overline{RESET}$ = 0 ⇒ Q = 0 (overrides clock).
n is time prior to clock.
n+1 is time following clock.

These buffer registers are arrays of ten clocked "D" flip-flops. The flip-flops are arranged as a dual 5 array (100000111 & 100000382) and single 10 arrays with reset (100000109 and 100000125).

The 100000111, 100000382 and 100000109 have true "D" inputs. The logic state presented at these "D" inputs will appear at the Q outputs after a negative transition of the clock. The 100000125 has complementing "D" inputs ("$\overline{D}$"). The logic state presented at these "$\overline{D}$" inputs will invert and appear at the Q outputs after a negative-going transition of the clock. The complementing input ("$\overline{D}$") permits the use of standard AND-OR-INVERT gates to achieve the AND-OR function without additional gate delays.

100000126

Pin Configuration



Triple 3-Input AND Gate

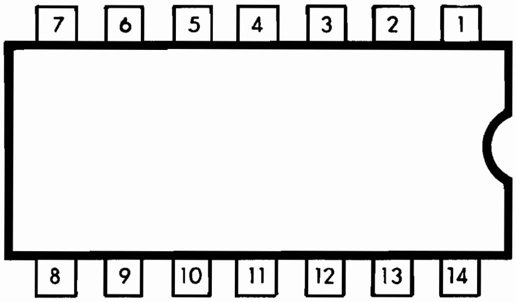
Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

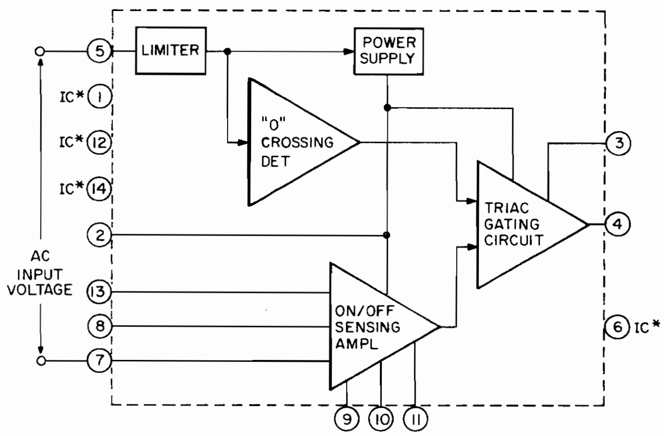
Positive logic: Y = ABC

100000127

Pin Configuration



Functional Block Diagram



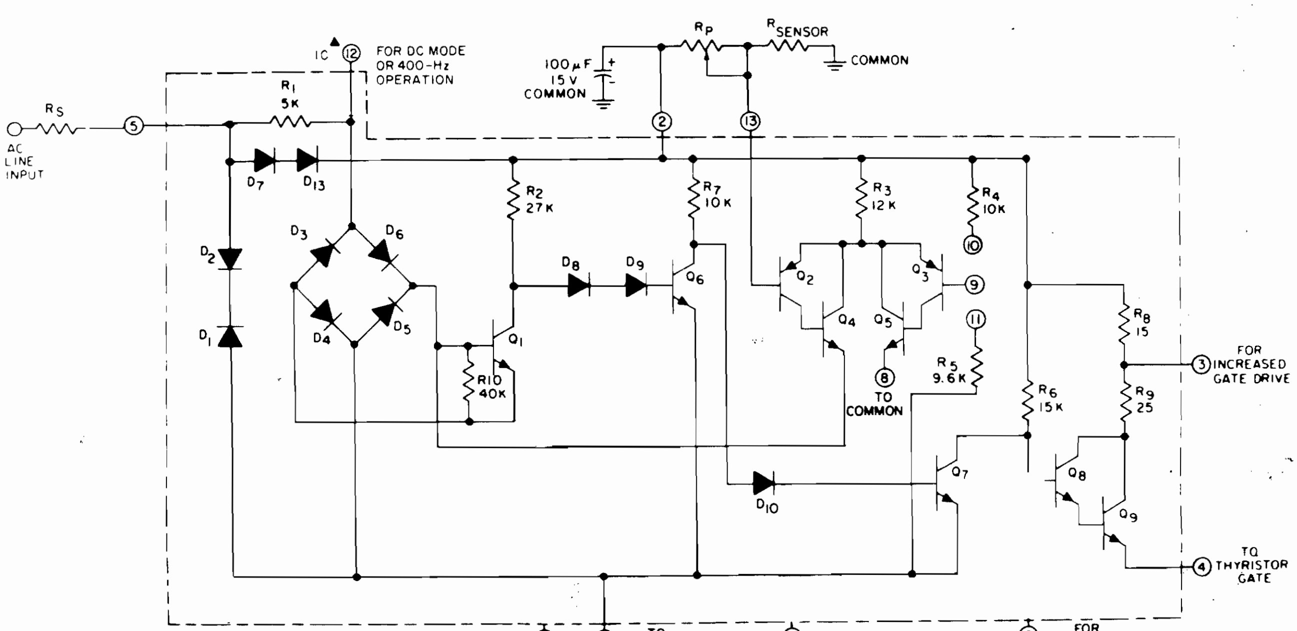
IC* = INTERNAL CONNECTION
DO NOT USE

Zero Voltage Switch

The 100000127 zero voltage switch is a monolithic integrated circuit designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24V, 120V, 208/230V and 277V at 50/60 and 400Hz. This switch incorporates four functional blocks:

1. Limiter-Power Supply -- permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier -- tests the condition of external sensors or command signals.
3. Zero-Crossing Detector -- synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point.
4. Triac Gating Circuit -- Provides high-current pulses to the gate of the power controlling thyristor.

Schematic



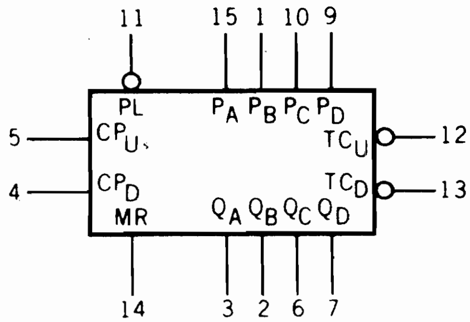
ALL RESISTANCE VALUES ARE IN OHMS

▲ IC=INTERNAL CONNECTION -- DO NOT USE

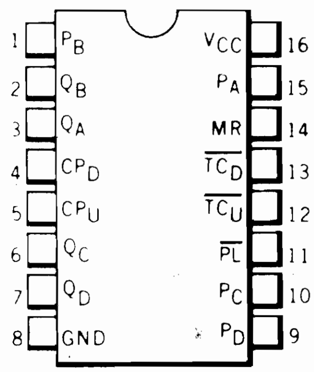
100000252 100000128 100000384

Up/Down Decade and Binary Counters

Logic Symbol

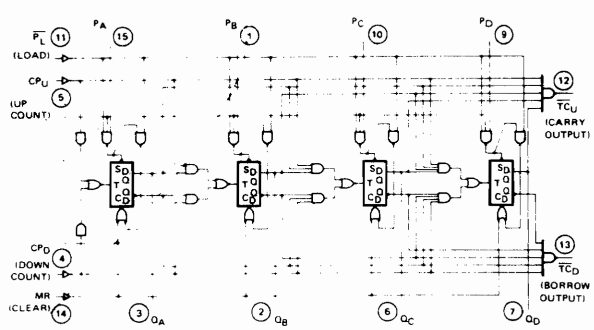


Pin Configuration

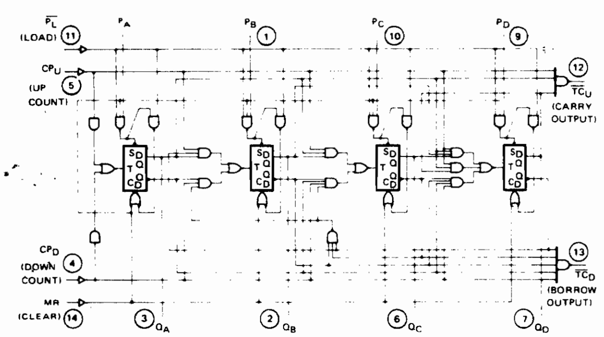


Logic Diagrams

100000128



100000252, 100000384



○ = PIN NUMBER

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Mode Selection
(Both Counters)

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

Notes:

H = High voltage level
L = Low voltage level
X = Don't care condition
CP = Clock pulse.

The 100000252 & 100000384 are synchronous Up/Down BCD Decade Counters and the 100000128 is a synchronous Up/Down 4-Bit Binary Counter. All these counters have separate up/down clocks, parallel load facility, terminal count outputs for multidecade operation and an asynchronous overriding master reset.

These counters can be reset, preset and count up or down. The operating modes are tabulated in the Mode Selection table. The operating modes of both devices are identical; the only difference between the devices is the count sequences.

Counting is synchronous, with the outputs changing state after the Low to High transition of either the Count-Up Clock (CP_U) or Count-Down Clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is High. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are Low simultaneously.) All counters will respond to a clock pulse on either input by changing to the next appropriate state of the count sequence. The state diagram for the 100000252 & 100000384 show the regular sequence and in addition shows the sequence of states if a code greater than nine is present in the counter.

Continued. . . .

100000252 100000128 100000384

Continued

Logic Equations for Terminal Count

100000252 , 100000384

$$TC_U = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot \overline{CP_U}$$

$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

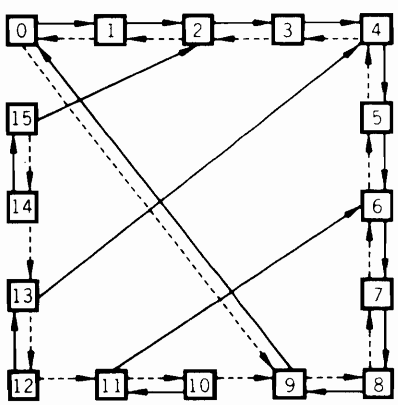
100000128

$$TC_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP_U}$$

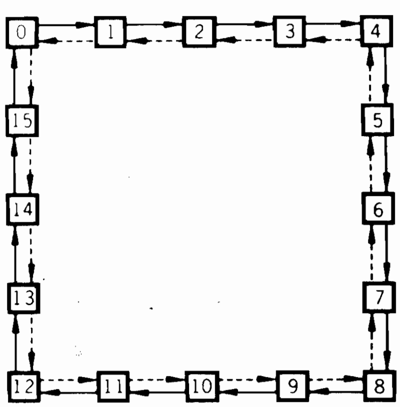
$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

State Diagrams

100000252 , 100000384



100000128



COUNT UP ————
COUNT DOWN -------

All counters have a parallel load (asynchronous) facility which permits the device to be preset. Whenever the parallel load ($\overline{PL}$) input is Low, and Master Reset is Low, the information present on the Parallel Data inputs (P_A, P_B, P_C, P_D) will be loaded into the counters and appear on the outputs independent of the conditions of the clock inputs. When the Parallel Load Input goes High, this information is stored in the counters and when the counters are clocked they change to the next appropriate state in the count sequence. The Parallel Data inputs are inhibited when the Parallel Load is High and have no effect on the counters.

The Terminal Count-Up ($\overline{TC_U}$) and Terminal Count-Down ($\overline{TC_D}$) outputs (carry and borrow, respectively) allow multidecade counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and terminal count-down clock input of the following counter.

The terminal count-up outputs are Low when their count-up clock inputs are Low and the counters are in state nine (100000252 & 100000384) and state fifteen (100000128). Similarly, the terminal count-down outputs are Low when their count-down clock inputs are Low and both counters are in state zero. Thus, when the 100000252 & 100000384 counters are in state nine and the 100000128 counter is in state fifteen and all are counting up, or all counters are in state zero and counting down, a clock pulse will change the counter's state on the rising edge and simultaneously clock the following counter through the appropriate active Low terminal count output. There are two gate delays per state when these counters are cascaded.

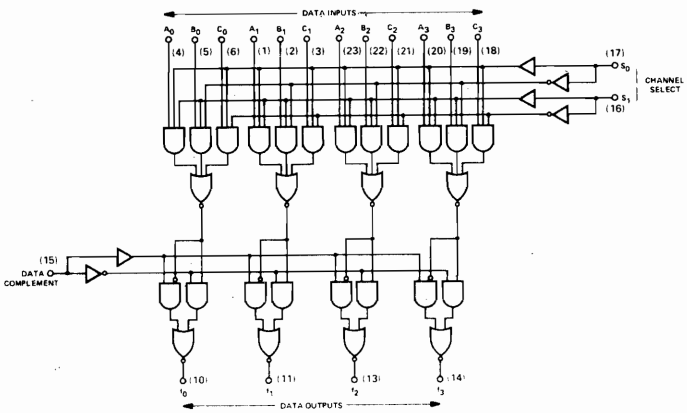
The asynchronous Master Reset input (MR), when High, overrides all input and clears the counters. Master reset overrides parallel load so that when both are activated the counters will be reset. (Obviously, both parallel load and master reset must not be deactivated simultaneously for predictable operation.)

100000129 100000044

Logic Diagrams

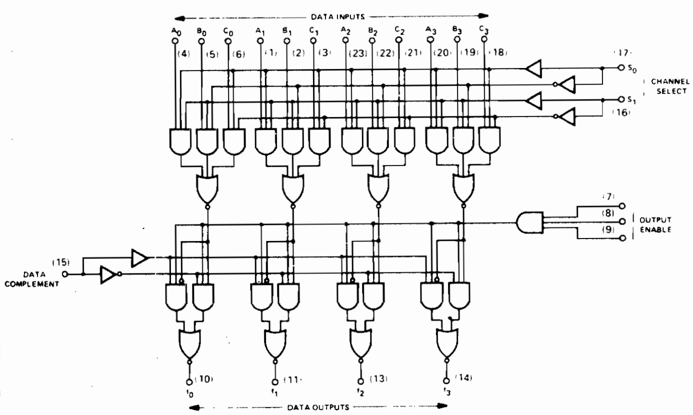
100000129

(Active Pull-up)



100000044

(Open Collector)



3-Input, 4-Bit Digital Multiplexer

Logic Diagram/Pin Designations

V_{CC} = Pin 24

Gnd = Pin 12

Truth Table

Data Input A_n B_n C_n	Channel Select S_0 S_1	Data Complement	Output Enable '044	Data Outputs
A_n x x	1 1	0	1	A_n
x B_n x	0 1	0	1	B_n
x x C_n	1 0	0	1	C_n
x x x	0 0	0	1	0
A_n x x	1 1	1	1	$\overline{A_n}$
x B_n x	0 1	1	1	$\overline{B_n}$
x x C_n	1 0	1	1	$\overline{C_n}$
x x x	0 0	1	1	1
x x x	x x	x	0	1

X = Either state.

The 3-input, 4-bit multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

The data complement input controls the conditional complement circuit at the multiplexer output to effect either inverting or non-inverting data flow.

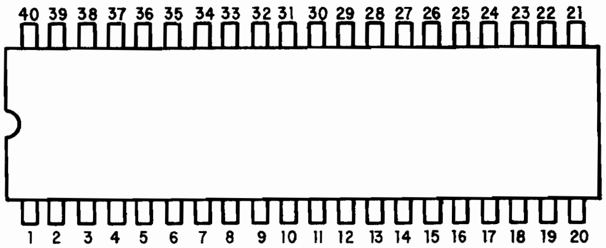
The 100000129 employs active output structures to effect minimum delays; the 100000044 utilizes bare collector outputs for expansion of input terms.

The 100000044 may be expanded by connecting its outputs to the outputs of another 100000044. Provision is made for use of a 3-bit code to determine which multiplexer is selected; thus, eight multiplexers may be commoned to effect a 4-pole, 24-position switch.

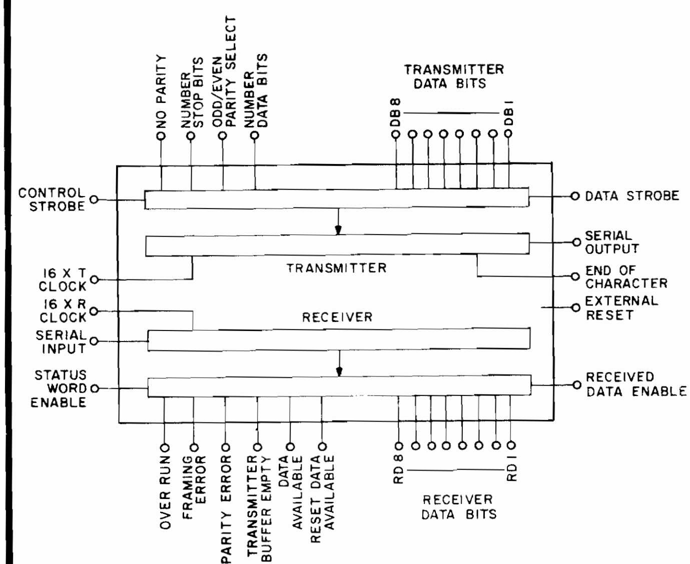
100000130 100000536

Asynchronous Receiver/Transmitter

Pin Configuration



Block Diagram



The Asynchronous Receiver/Transmitter is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits and either odd/even parity or no parity. The baud rate (bits per word), parity mode and the number of stop bits are externally selectable.

Description of Pin Functions

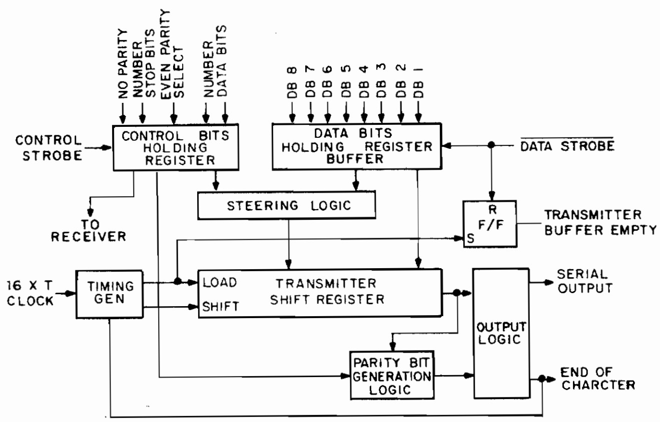
Pin No.	Name	Symbol	Function
1	V_{cc} Power Supply	V_{cc}	+5V Supply
2	V_{gg} Power Supply	V_{gg}	-12V Supply
3	Ground	V_{gr}	Ground
4	Received Data Enable	$\overline{RDE}$	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits	RD8-RD1	These are the 8 data output lines. Received characters are right justified, the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when RDE is "0" and a high impedance state when RDE is "1". Thus, the data output lines can be bus structure oriented.
13	Receive Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected POE.
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit.
15	Over-Run	OR	This line goes to a logic "1" if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver holding register.
16	Status Word Enable	$\overline{SWE}$	A logic "0" on this line places the status word bits (PE, FE, OR, DA, TBMT) onto the output lines. These are tri-state also.
17	Receiver Clock	RCP	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	Reset Data Available	$\overline{RDA}$	A logic "0" will reset the DA line.
19	Receive Data Available	DA	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register.
20	Serial Input	SI	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception.
21	External Reset	XR	Resets all registers. Sets SO, EOC, and TBMT to a logic "1".
22	Transmitter Buffer Empty	TBMT	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character.
23	Data Strobe	$\overline{DS}$	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS.
24	End of Character	EOC	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character.
25	Serial Output	SO	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted.

Continued ....

100000130 100000536

Continued

Transmitter Block Diagram

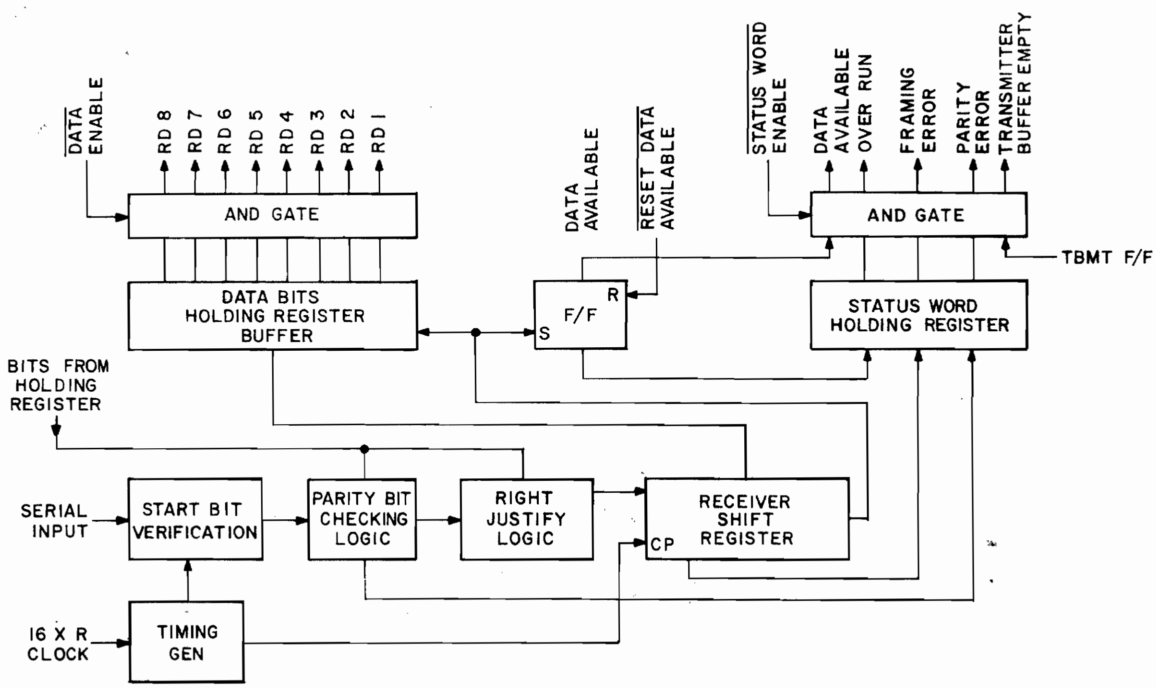


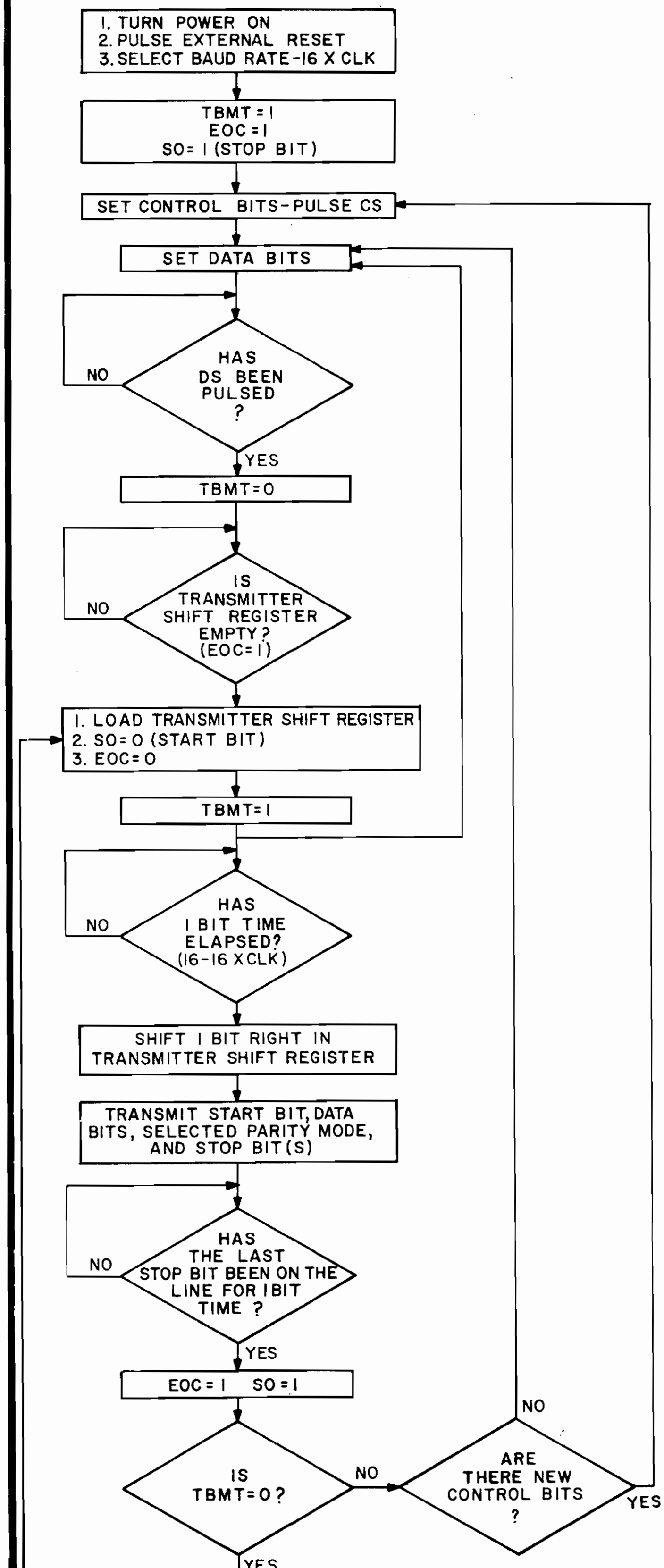
Description of Pin Functions (Continued)

Pin No.	Name	Symbol	Function
26-33	Data Bit Inputs	DB1-DB8	There are up to 8 data bit input lines available.
34	Control Strobe	CS	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity	NP	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits	TSB	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Bits Character	NB2, NB1	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits character. NB1 NB2 Bits Character 0 0 5 1 0 6 0 1 7 1 1 8
39	Odd Even Parity	EPS	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock Line	TCP	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

Continued....

Receiver Block Diagram





Transmitter Operation

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBMT, EOC and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once data strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering, (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously mentioned.

Continued. . . .

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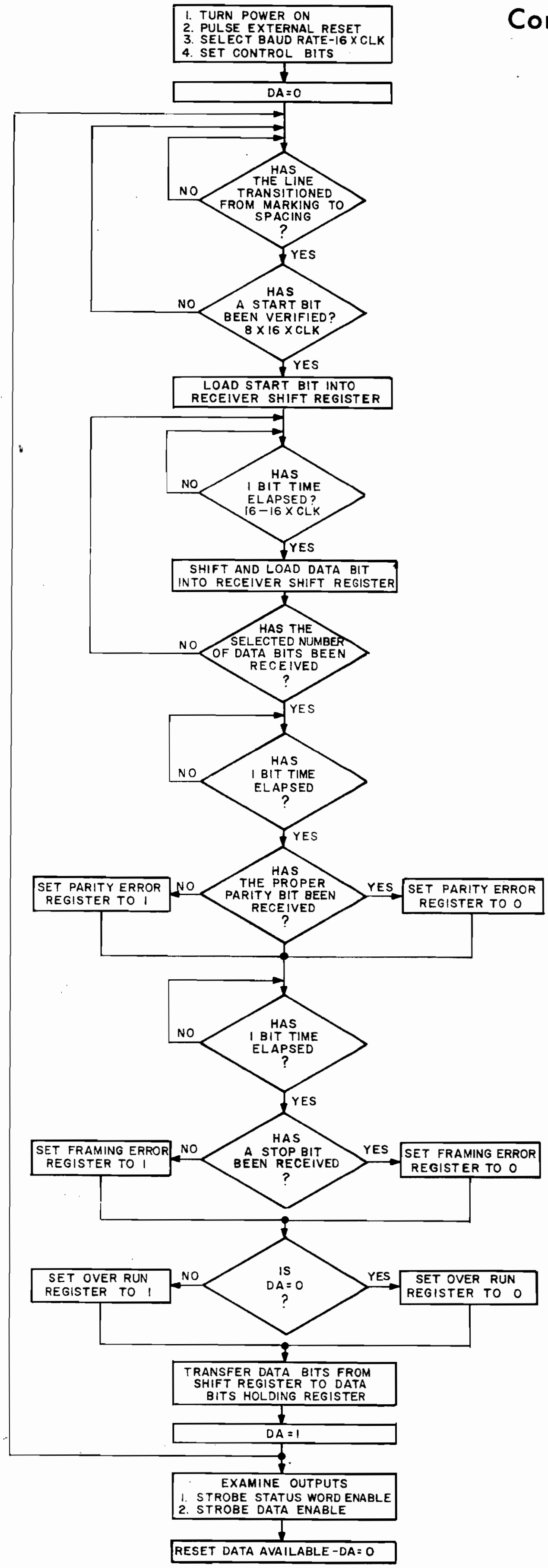
Continued



Receiver Operation

Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DA) to a logic "0".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16X clock is in a logic "1" state, the bit time for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip-flop and/or the framing error flip-flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditioning set to a logic "0".

Once a full character is received, internal logic looks at the data available (DA) signal to determine if data has been read out. If the DA signal is at a logic "1" the receiver will assume data has not been read out and the overrun flip-flop of the status word holding register will be set to a logic "1". If the DA signal is at a logic "0" the receiver will assume that data has been read out. After DA goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

Continued. . . .

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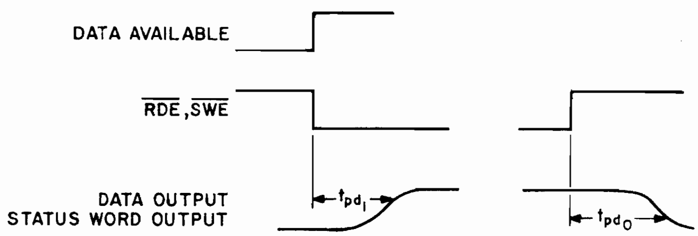
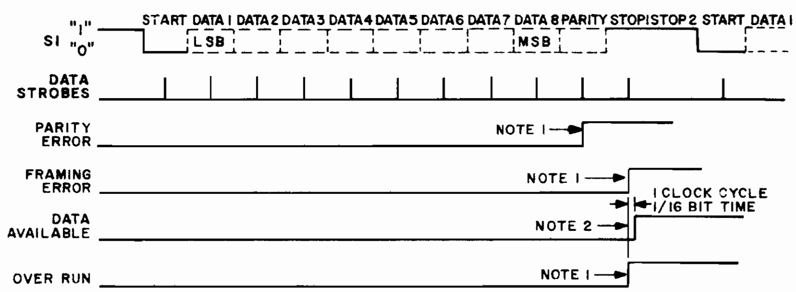
Continued

Receiver Propagation Delay Timing Diagram



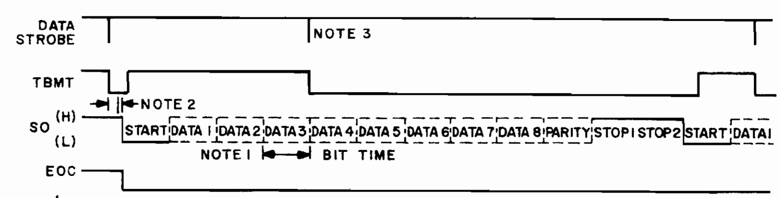
Receiver Timing Diagram



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE DETECTED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGH JUSTIFIED*; THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

Transmitter Timing Diagram



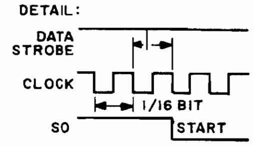
NOTE: TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1.

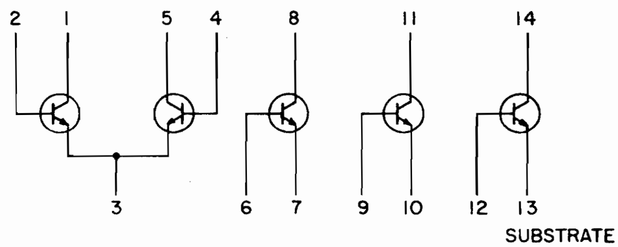
DETAIL:



100000131

General Purpose Transistor Array

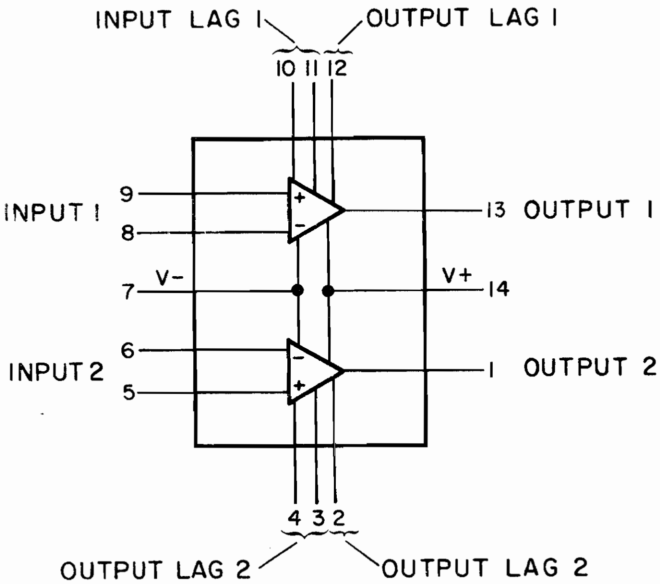
Schematic



100000132

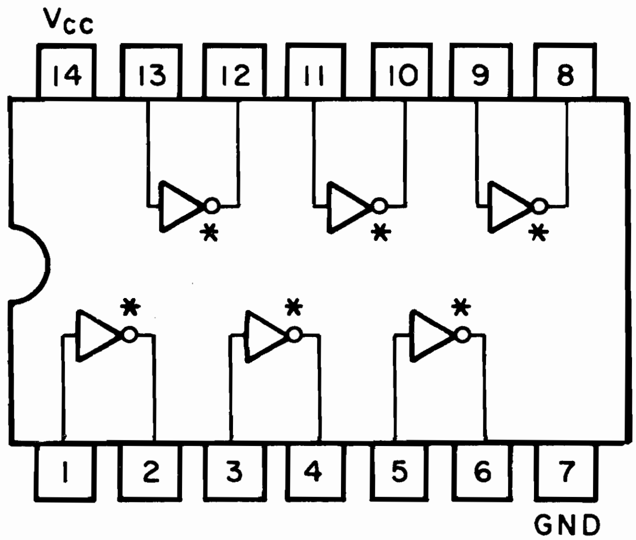
Dual Stereo Preamplifier

Pin Configuration



100000133

Pin Configuration



DIP (TOP VIEW)

*Open collector

Hex Inverter

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Positive logic: $Y = \overline{A}$

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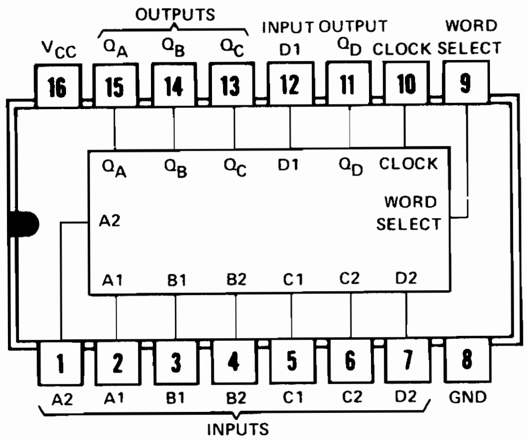
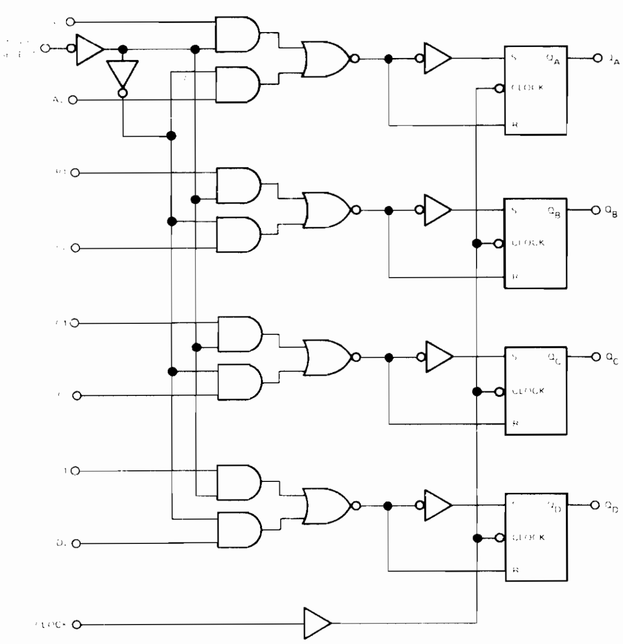
100000134

Pin Configuration



Logic Diagram



4-Bit Data Selector/Storage Register

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Positive logic: word select low for word 1, word select high for word 2.

This monolithic data selector/storage register is composed of four S-R master-slave flip-flops, four AND-OR-INVERT gates, one buffer and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

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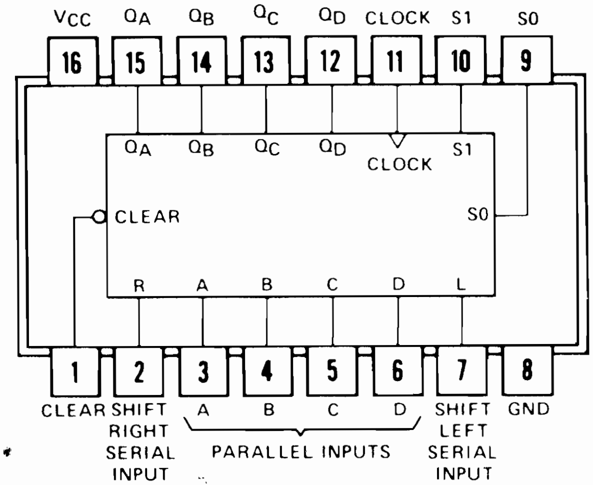
4-Bit Bidirectional Universal Shift Registers

Pin Configuration



Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Function Table

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S_1	S_0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state).

L = low level (steady state).

X = irrelevant (any input, including transitions).

↑ = transition from low to high level.

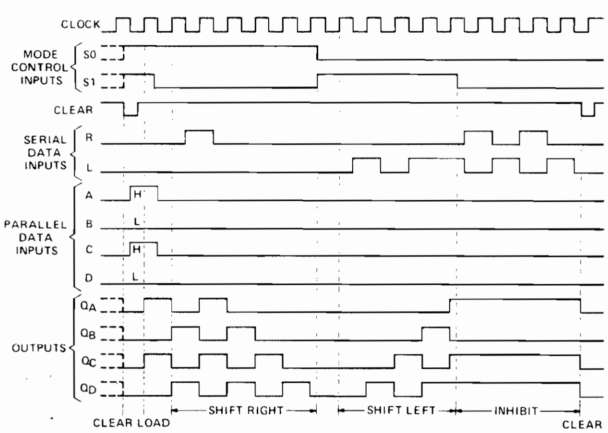
a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the most recent ↑ transition of the clock.

Note: The 100000234 is a Schottky device.

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences



The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

- Parallel (Broadside) Load
- Shift Right (in the direction Q_A toward Q_D)
- Shift Left (in the direction Q_D toward Q_A)
- Inhibit Clock (Do nothing)

Continued....

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Continued

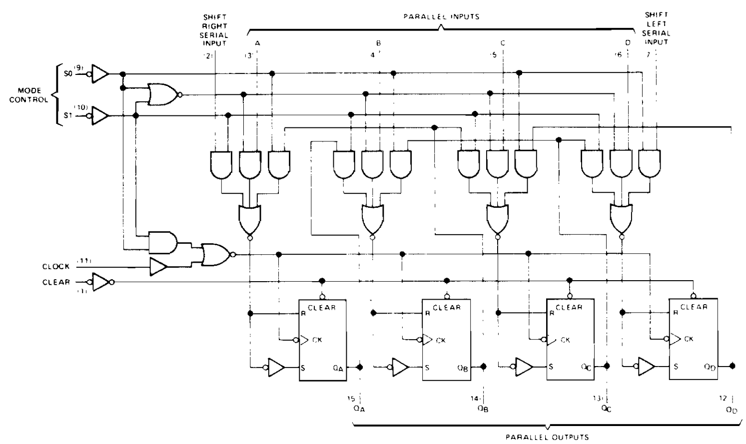
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

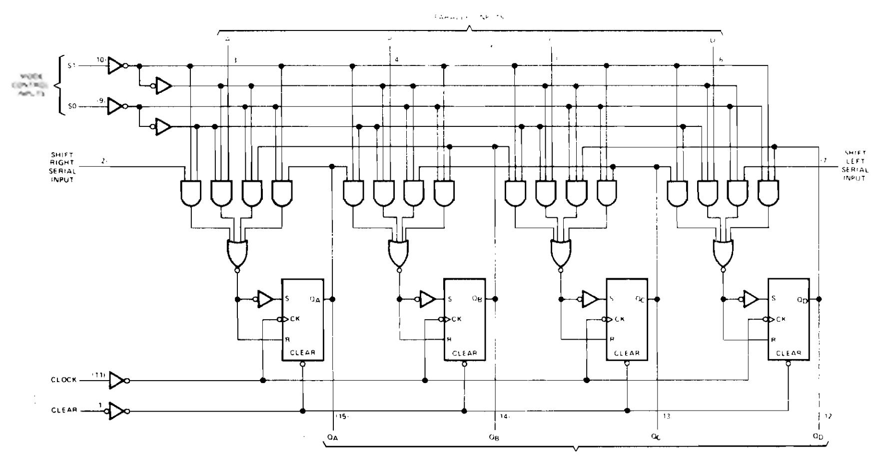
Clocking of the flip-flop is inhibited when both mode control units are low. The mode controls of the 100000135 should be changed only while the clock input is high.

Logic Diagrams

100000135



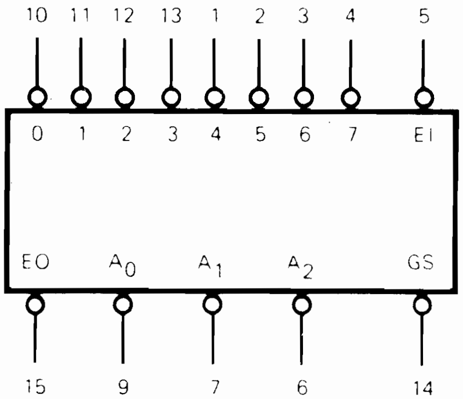
100000234



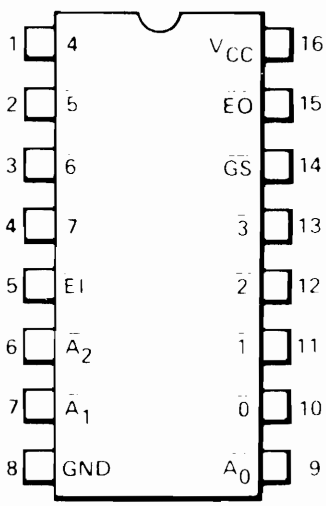
⊲▷ . . . . dynamic input activated by a transition from a high level to a low level.

100000136

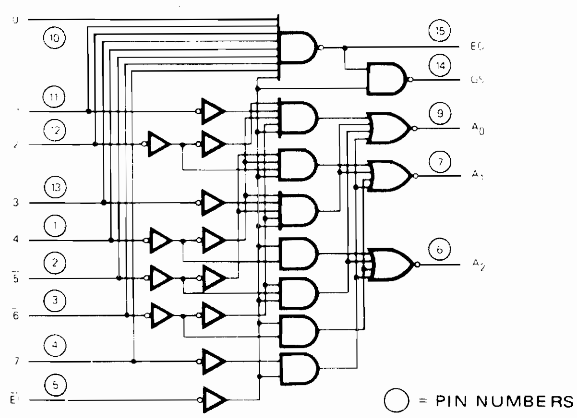
Logic Symbol



Pin Configuration



Logic Diagram



Eight-Input Priority Encoder

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

$\overline{0}$ .... Priority (Active LOW) Input
$\overline{1}$ to $\overline{7}$ .... Priority (Active LOW) Inputs
$\overline{EI}$ .... Enable (Active LOW) Input
$\overline{EO}$ .... Enable (Active LOW) Output
$\overline{GS}$ .... Group Select (Active LOW) Output
$\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$. Address (Active LOW) Outputs

Truth Table

$\overline{EI}$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{GS}$	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

The 100000136 is a multipurpose 8-input priority encoder designed to accept data from eight active LOW inputs and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority.

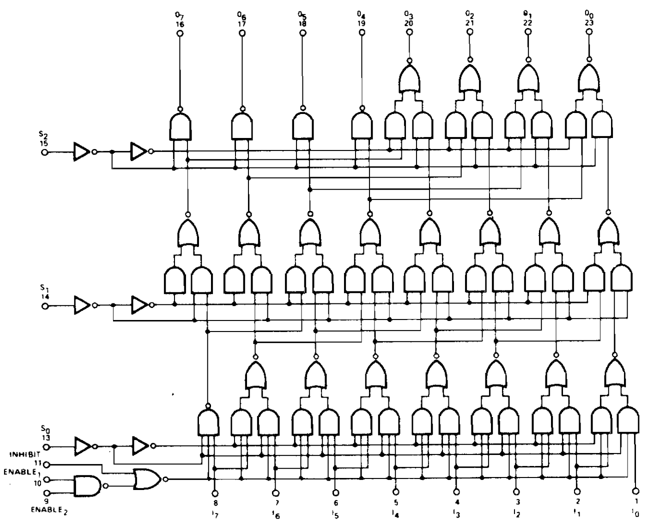
A HIGH on the Input Enable ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

A Group Signal output ($\overline{GS}$) and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active level LOW when any input is LOW; this indicates when any input is active. The $\overline{EO}$ is active level LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are inactive HIGH when the input enable is HIGH.

100000137

8-Bit Position Scaler

Logic Diagram



NOTE: All inputs have diode clamps.

Logic Diagram/Pin Designations

V_{CC} = Pin 24
Gnd = Pin 12

Truth Table

INHIBIT	ENABLE 1 & 2	S_0	S_1	S_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	1	0	0	0	I_0	I_1	I_2	$\bar{I}_3$	$\bar{I}_4$	I_5	$\bar{I}_6$	I_7
0	1	1	0	0	$\bar{I}_1$	$\bar{I}_2$	$\bar{I}_3$	I_4	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1
0	1	0	1	0	$\bar{I}_2$	I_3	$\bar{I}_4$	I_5	$\bar{I}_6$	$\bar{I}_7$	1	1
0	1	1	1	0	I_3	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1	1
0	1	0	0	1	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1	1	1
0	1	1	0	1	I_5	$\bar{I}_6$	$\bar{I}_7$	1	1	1	1	1
0	1	0	1	1	I_6	$\bar{I}_7$	1	1	1	1	1	1
0	1	1	1	1	I_7	1	1	1	1	1	1	1
1	X	X	X	X	1	1	1	1	1	1	1	1
X	0	X	X	X	1	1	1	1	1	1	1	1

Note:

X indicates either logic "1" or logic "0" may be present.

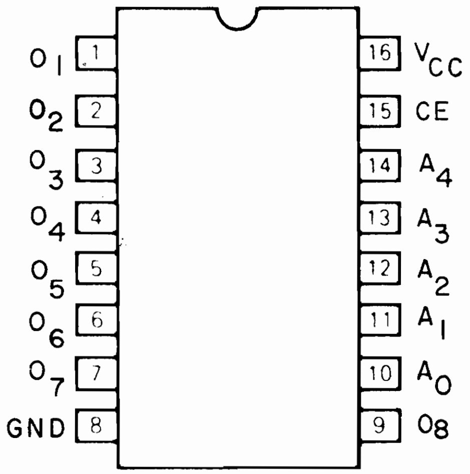
The 8-bit position scaler is an MSI array of approximately 70 gate complexity. The primary function of this device is to scale (or shift) data bit positions by a selection of a 3-bit binary selector code.

The most significant bit input (I_7) may be shifted 8 positions to the least significant bit output (O_0). At zero shift, or scale select, all eight input data bits are transferred and inverted to their respective outputs, (I_0 to O_0, I_1 to O_1, I_2 to O_2, etc.) At a shift, or scale select, of one, each input bit (I_n) will shift to the next lower output bit (O_{n-1}). See truth table for other shift codes.

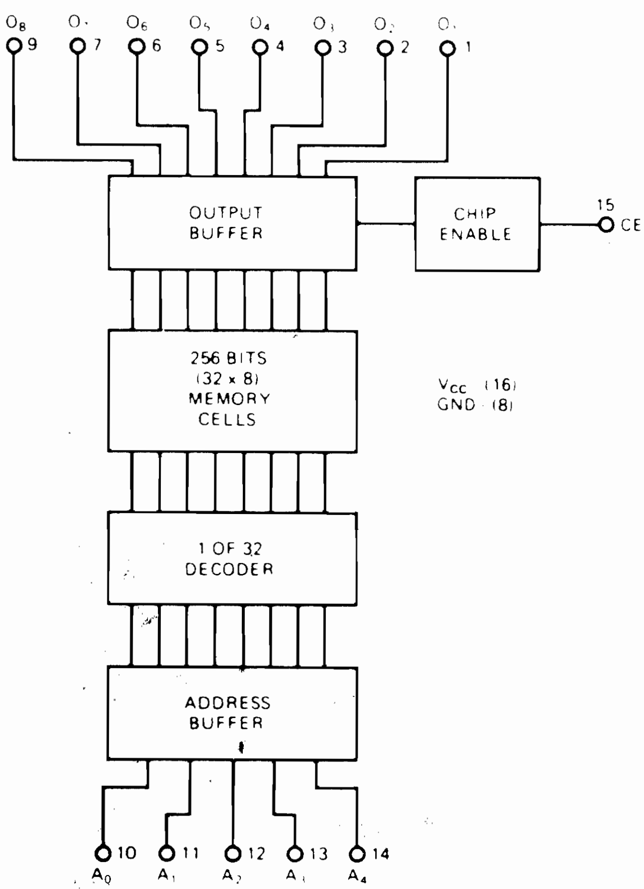
REV. 03

100000140 100000141 100000142 100000148 100000149 100000215 100000216 100000217 100000218 100000219 100000269 100000270 100000271 100000272 100000273 100000274 100000275 100000276 100000277 100000278 100000279 100000280 100000499 100000500

Pin Configuration



Functional Block Diagram



256-Bit Bipolar Read Only Memory

Logic Diagram/Pin Designations

V_{CC} = Pin 16

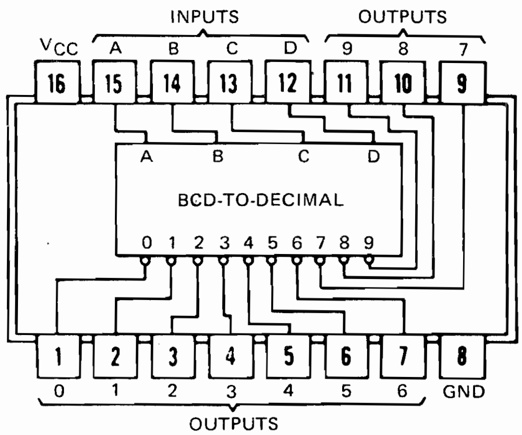
Gnd = Pin 8

These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

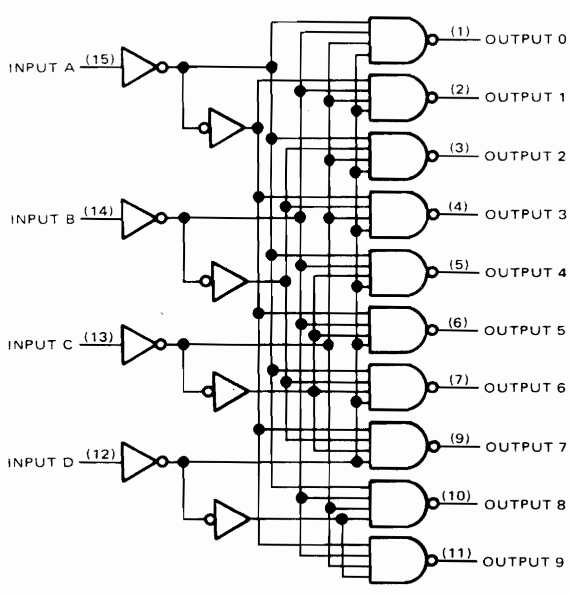
Memory expansion is simple; three-state outputs are provided on the 100000215; uncommitted collector outputs are provided on all other devices. Each device has on-chip address decoding and chip enable. The memory is fabricated with all logic level zeroes(low); logic level ones (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

100000143

Pin Configuration



Logic Diagram



BCD-To-Decimal Decoder-Driver

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Function Table

	Inputs				Outputs									
No.	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
Invalid	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off); L = low level (on).

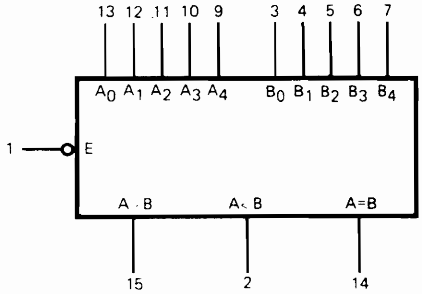
This monolithic BCD-to-decimal decoder/driver consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions.

REV. 03

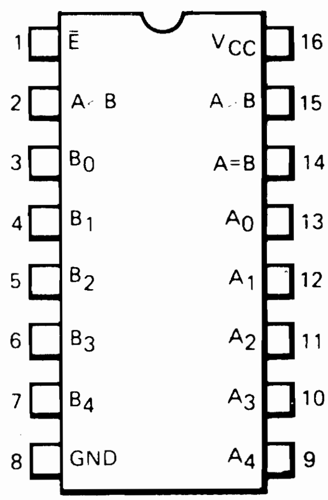
100000144

5-Bit Comparator

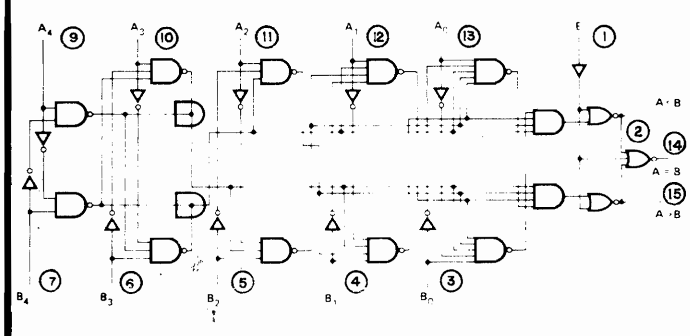
Logic Symbol



Pin Configuration



Logic Diagram



○ = PIN NUMBERS

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

Ē .... Enable (Active LOW) Input

A_0, A_1, A_2, A_3, A_4.... Word A Parallel Inputs

B_0, B_1, B_2, B_3, B_4.... Word B Parallel Inputs

A < B .... A Less Than B Output

A > B .... A Greater Than B Output

A = B .... A Equal to B Output

Truth Table

Ē	Ay		By	A<B	A>B	A=B
H	X		X	L	L	L
L	Word A	=	Word B	L	L	H
L	Word A	>	Word B	L	H	L
L	Word B	>	Word A	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Voltage Level

The 100000144 is a high speed expandable comparator which provides comparison between two 5-bit words and gives three outputs, "less than", "greater than" and "equal to". A HIGH level on the active LOW enable input forces all three outputs LOW.

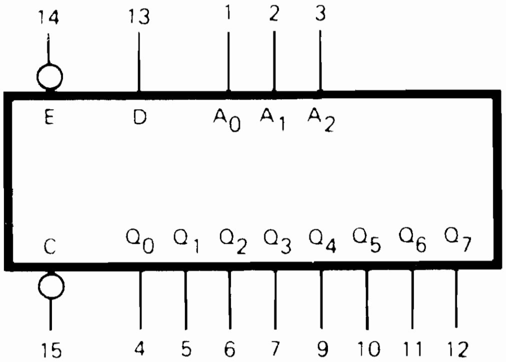
This 5-bit comparator uses combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable input (Ē).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion.

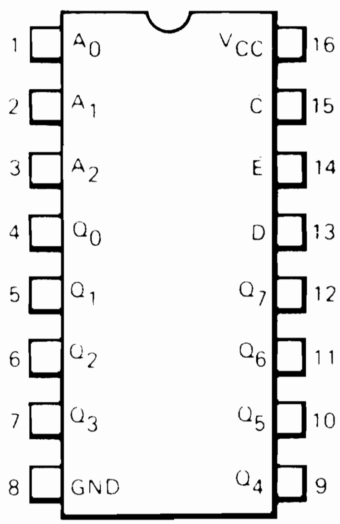
The A_4 and B_4 inputs are the most significant inputs, and A_0 and B_0 are the least significant. Thus, if A4 is HIGH and B4 is LOW, the A > B output will be HIGH regardless of all other inputs except Ē.

100000145

Logic Symbol



Pin Configuration



8-Bit Addressable Latch

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

A_0, A_1, A_2..... Address Inputs
D.............. Data Input
$\overline{E}$.............. Enable (Active LOW) Input
$\overline{C}$.............. Clear (Active LOW) Input
Q_0 to Q_7........ Parallel Latch Outputs

Truth Table

Present Output States

$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Mode
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
.	.	.		.					.					
.	.	.		.					.					
.	.	.		.					.				.	
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					Addressable Latch
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
.	.	.		.				.						
.	.	.		.				.						
.	.	.		.				.						
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State

Mode Selection

$\overline{E}$	$\overline{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

The 100000145 is a high speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active level LOW common clear for resetting all latches as well as an active level LOW enable.

This latch has four modes of operation, which are shown in the mode selection table. In the addressable latch mode, data on the data line (D)

Continued ....

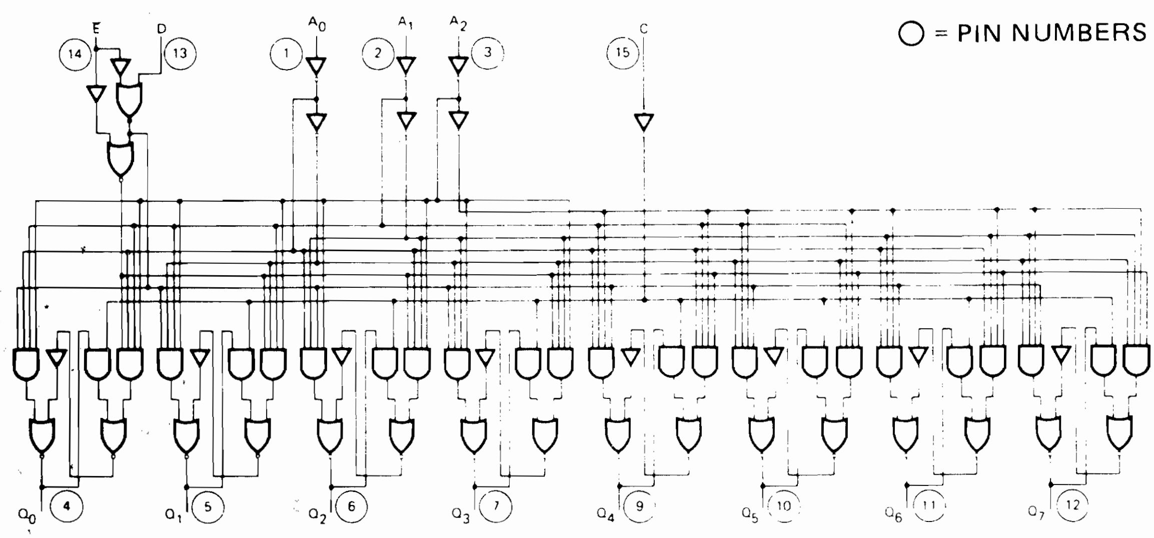
100000145
Continued

is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating this device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

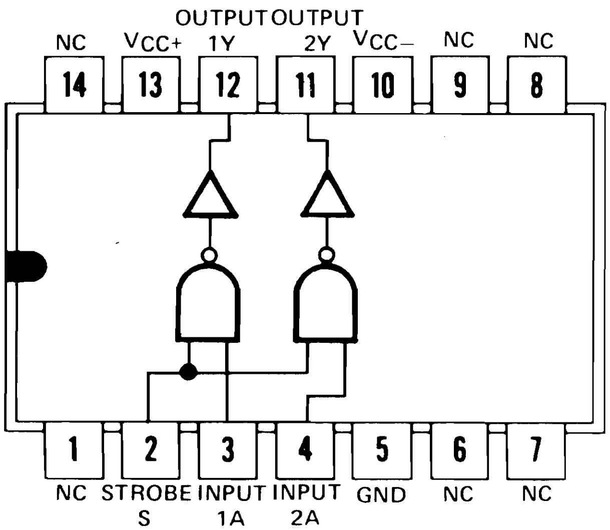
Logic Diagram



100000146

Dual Line Driver

Pin Configuration



Pin Designations

V_{CC+} = Pin 13

V_{CC-} = Pin 10

Gnd = Pin 5

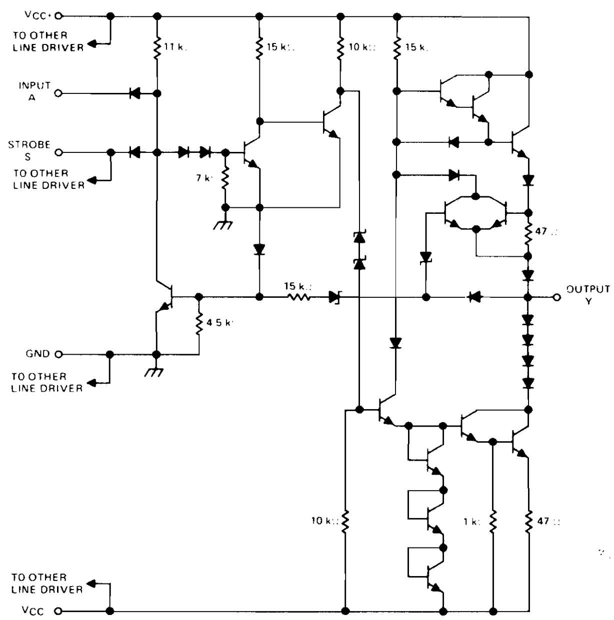
NC = No Internal Connection

Positive logic: Y = $\overline{AS}$

This device is a monolithic dual line driver which satisfies the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C.

A rate of 20, 000 bits per second can be transmitted with a full 2500pF load.

Schematic (Each Line Driver)

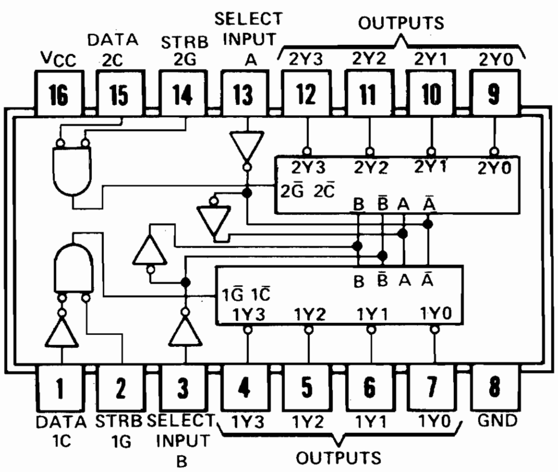


Component values shown are nominal.

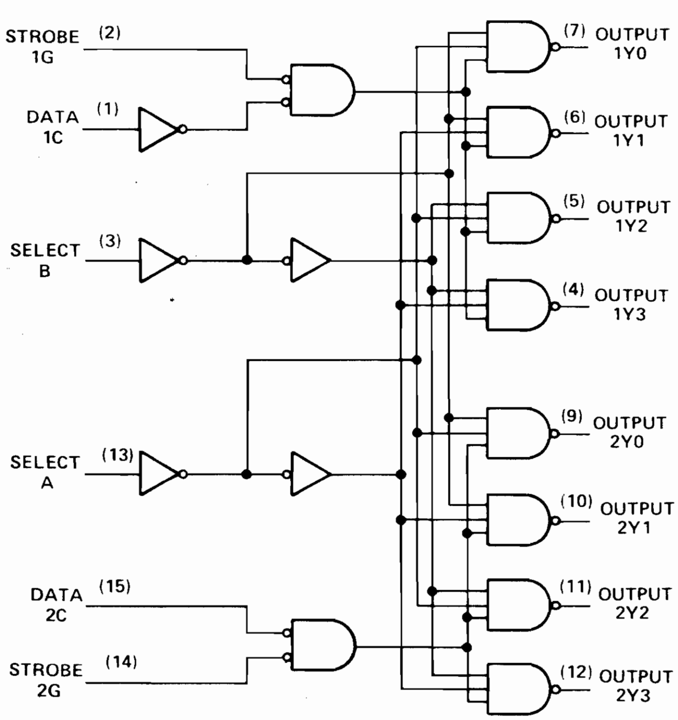
100000147

Dual 2-Line-To-4-Line Decoder/Demultiplexer

Pin Configuration



Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Function Tables
2-Line-To-4-Line Decoder or 1-Line-To-4-Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

Function Table
3-Line-To-8-Line Decoder or 1-Line-To-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C*	B	A	G**	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Notes: *C = inputs 1C and 2C connected together.
**G = inputs 1G and 2G connected together.
H = high level, L = low level,
X = irrelevant.

The 100000147 monolithic TTL circuit features dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections

Continued ....

100000147

Continued

are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided to minimize transmission-line effects and simplify system design.

100000140 100000141 100000142 100000148 100000149 100000215 100000216 100000217 100000218 100000219 100000269 100000270 100000271 100000272 100000273 100000274 100000275 100000276 100000277 100000278 100000279 100000280 100000499 100000500

256-Bit Bipolar Read Only Memory

Logic Diagram/Pin Designations

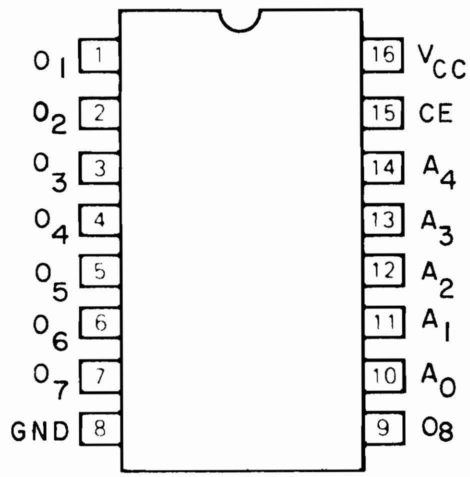
V_{CC} = Pin 16

Gnd = Pin 8

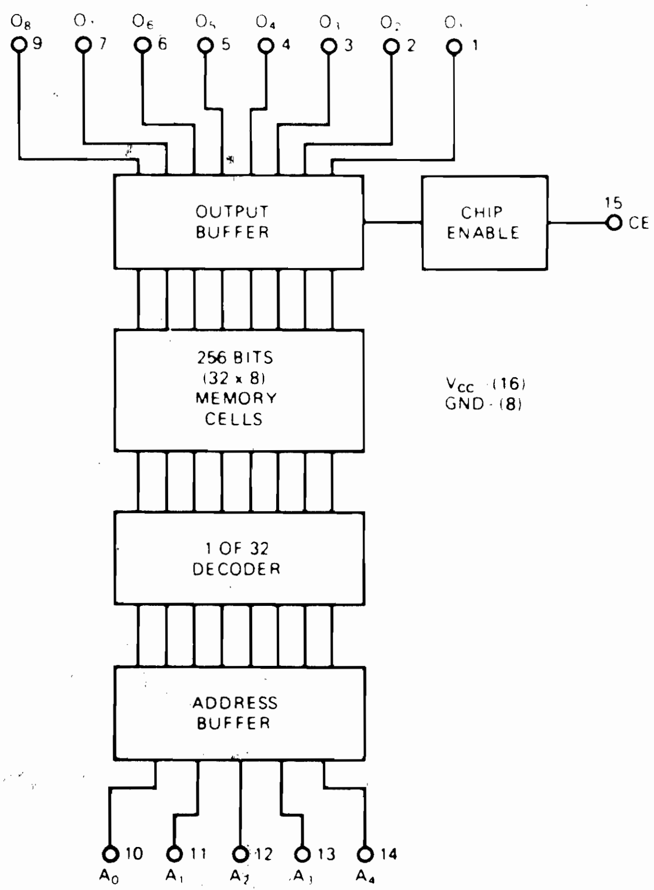
These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

Memory expansion is simple; three-state outputs are provided on the 100000215; uncommitted collector outputs are provided on all other devices. Each device has on-chip address decoding and chip enable. The memory is fabricated with all logic level zeroes(low); logic level ones (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

Pin Configuration



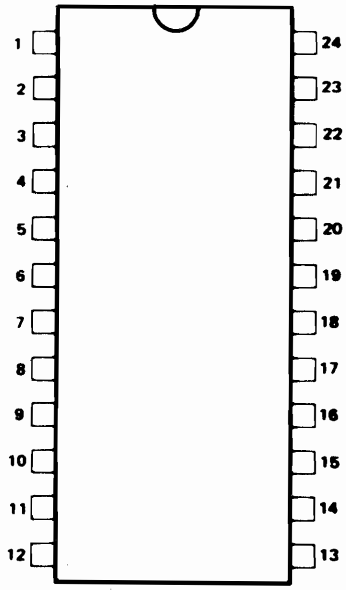
Functional Block Diagram



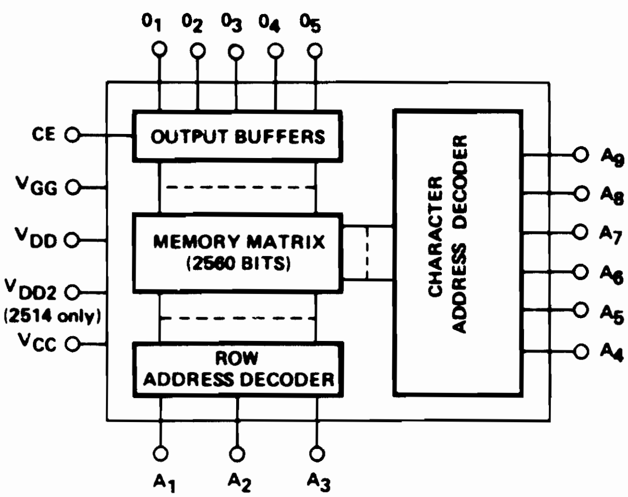
100000150

High Speed 64 X 7 X 5 Character Generator

Pin Configuration



Block Diagram



CE	OUTPUT
0	DATA
1	OPEN

Pin Designations

1.	V_{GG}	24.	V_{CC}
2.	NC	23.	NC
3.	NC	22.	Address 9
4.	Out 1	21.	Address 8
5.	Out 2	20.	Address 7
6.	Out 3	19.	Address 6
7.	Out 4	18.	Address 5
8.	Out 5	17.	Address 4
9.	NC	16.	Address 3
10.	Ground	15.	Address 2
11.	Chip Enable	14.	Address 1
12.	V_{DD}	13.	NC

Character Format

Row Address

A_3	A_2	A_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Character Address

	A_4	A_5	A_6	A_7	A_8	A_9
ASCII Character	1	1	0	0	1	0

The 100000150 is a high speed 2560-bit static ROM. The 64x7x5 character organization is formed on a 64x8x5 field.

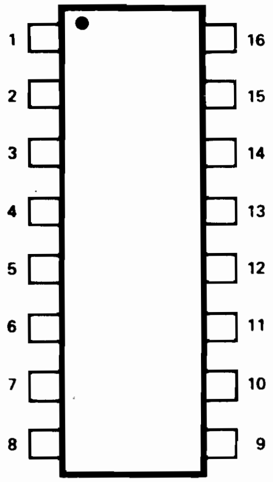
The product uses +5V, -5V and -12V power supplies, 5V TTL level input signals and tri-state outputs.

REV. 03

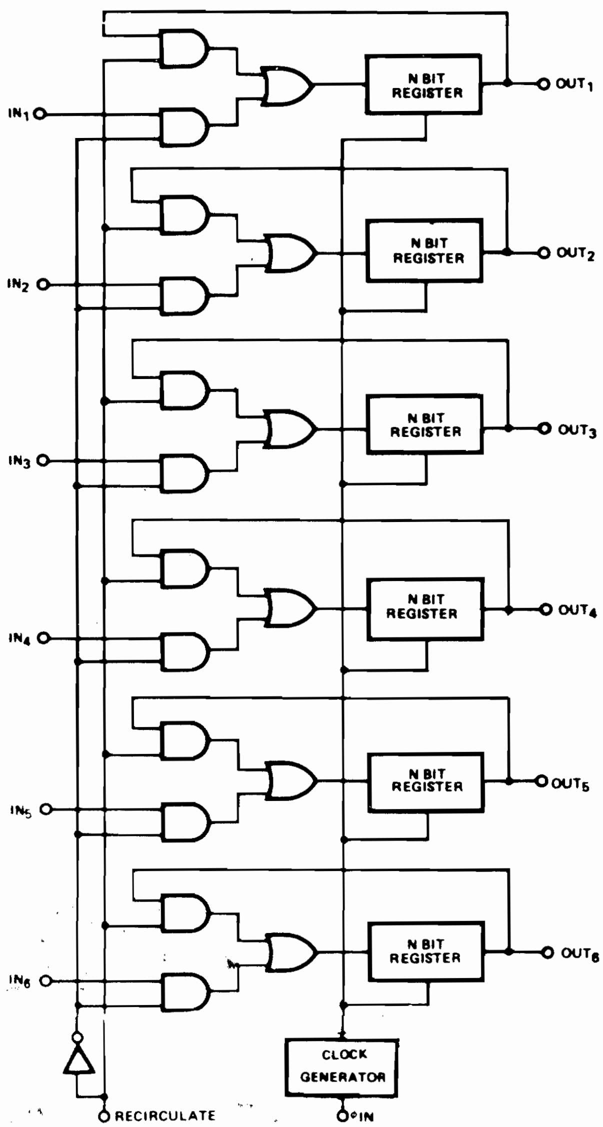
100000151

Hex 40-Bit Static Shift Register

Pin Configuration



Functional Block Diagram



Pin Designations

1. IN_4	16. V_{CC}
2. IN_5	15. IN_3
3. IN_6	14. IN_2
4. Recirculate	13. IN_1
5. V_{GG}	12. OUT_1
6. Clock	11. OUT_2
7. OUT_6	10. OUT_3
8. OUT_5	9. OUT_4

Truth Table

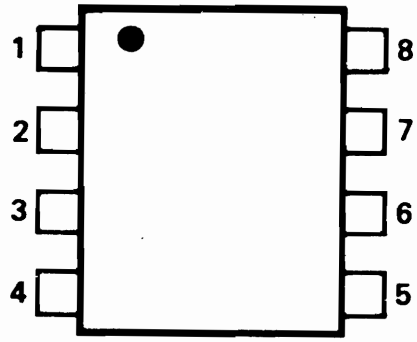
Recirculate	Input	Function
1	0	Recirculate
1	1	Recirculate
0	0	"0" is Written
0	1	"1" is Written

The Hex 40-bit recirculating static shift register consists of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for interfacing capability.

100000152

1024-Bit Recirculating Dynamic Shift Register

Package



Pin Designations

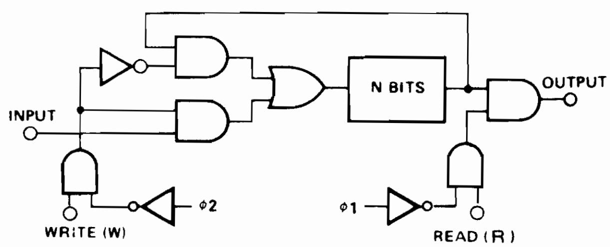
1. 0_2 Input clock
2. Output
3. Read
4. V_{DD}
5. Write
6. Input
7. 0_1 Output clock
8. V_{CC}

Truth Table

Write	Read	Function
0	0	Recirculate, Output is "0"
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is "0"
1	1	Read Mode, Output is Data

The 1024 bit recirculating dynamic shift register consists of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

Block Diagram

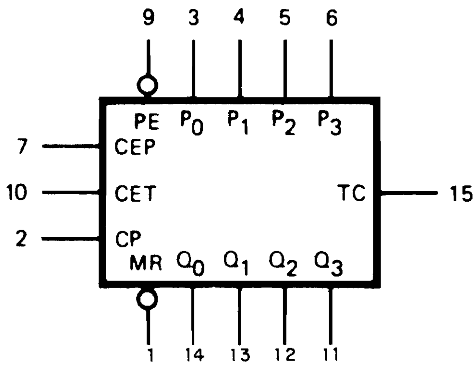


NOTE:
N = 1024 '0' = 0V, '1' = +5V

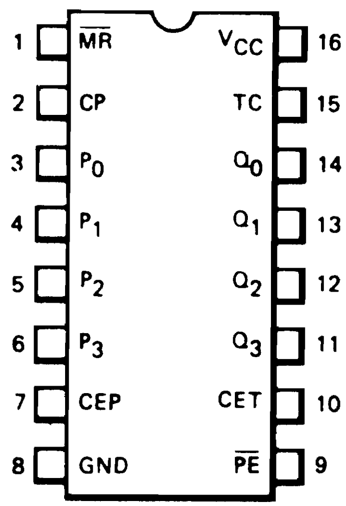
100000153 100000047

BCD Decade Counter-4 Bit Binary Counter

Logic Symbol

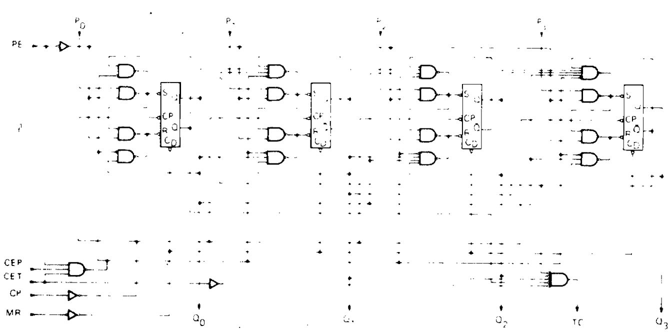


Pin Configuration

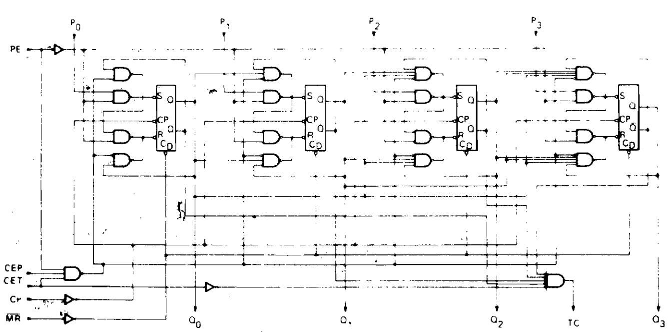


Logic Diagrams

100000153



100000047



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

$\overline{PE}$ .... Parallel Enable (Active LOW) Input

P_0, P_1, P_2, P_3 .. Parallel Inputs

CEP .... Count Enable Parallel Input

CET .... Count Enable Trickle Input

CP.............. Clock (Active HIGH Going Edge) Input

$\overline{MR}$ .... Master Reset (Active LOW) Input

Q_0, Q_1, Q_2, Q_3 .. Parallel Outputs

TC.............. Terminal Count Outputs

Mode Selection

$\overline{PE}$	CEP	CET	Mode
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH)

Terminal Count Generation

CET	100000153 ($Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3$)	100000047 ($Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$)	TC
L	L	L	L
L	H	H	L
H	L	L	L
H	H	H	H

$TC = CET \cdot Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3$ (100000153)

$TC = CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$ (100000047)

Positive Logic:

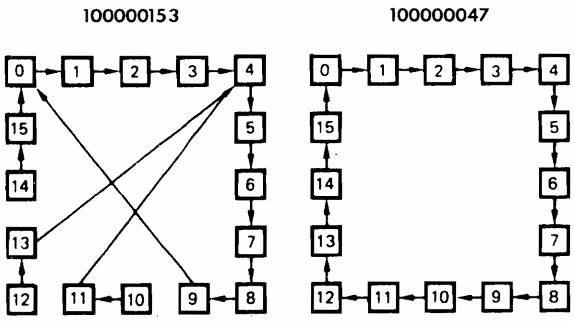
H = HIGH Voltage Level
L = LOW Voltage Level

The 100000153 is a high speed BCD decade counter, and the 100000047 is a high speed binary counter. Both counters are fully synchronous with the clock pulse driving four master/slave flip-flops in parallel through a clock buffer. During the

Continued ...

100000153 100000047

Continued



Logic Equations

Count Enable = CEP · CET · PE
TC for 100000153 = $CET \cdot Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3$
TC for 100000047 = $CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$
Preset = $\overline{PE}$ · CP + (rising clock edge)
Reset = $\overline{MR}$

Note: The 100000153 can be preset to any state but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

LOW to HIGH transition of the clock, the master is inhibited from further change. After the masters are locked out, data is transferred from the master to the slaves and reflected at the outputs. When the clock is HIGH, the masters are inhibited and the master/slave data path remains established. During the HIGH to LOW transition of the clock, the slave is inhibited from further change, followed by the enabling of the masters for the acceptance of data from the counting logic or the parallel entry logic.

The three control inputs, Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP), and Count Enable Trickle (CET), select the mode of operation. When the conditions for counting are satisfied, the rising edge of a clock pulse will change the counters to the next state of the count sequence shown in the State Diagram. The Count Mode is enabled when CEP and CET inputs and $\overline{PE}$ are HIGH.

These devices can be synchronously preset from the four Parallel inputs (P_{0-3}) when $\overline{PE}$ is LOW. When the Parallel Enable and Clock are LOW, each master of the flip-flops is connected to the appropriate parallel input (P_{0-3}) and the slaves (outputs) are steady in their previous state. When the clock goes HIGH, the masters are inhibited and this information is transferred to the slaves and reflected at the outputs. The parallel enable input overrides both count enable inputs, presetting the counter when LOW.

Terminal count is HIGH when the counter is at terminal count (state 9 for 100000153 and state 15 for 100000047), and Count Enable Trickle is HIGH, as shown in the logic equations.

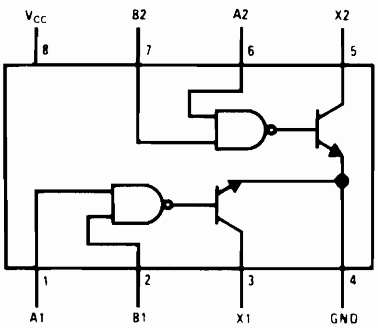
When LOW, the asynchronous master reset overrides all other inputs resetting the four outputs LOW.

Conventional operation, as shown in the Mode Selection table, requires that the mode control inputs ($\overline{PE}$, CEP, CET) are stable while the clock is LOW.

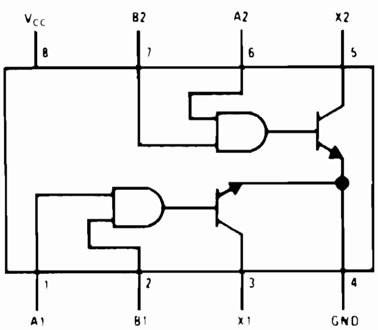
100000228 100000247 100000238 100000154 100000117

Dual Peripheral Drivers

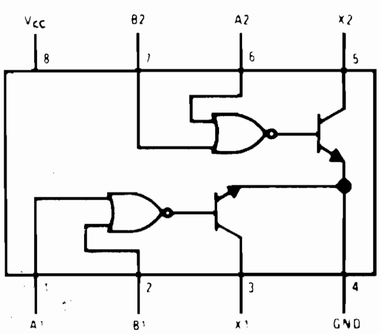
Pin Configurations



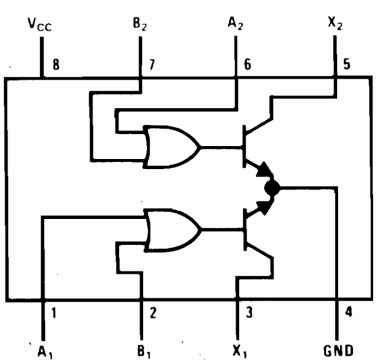
100000247/100000238



100000154



100000117



100000228

V_{CC} = Pin 8
Gnd = Pin 4

Truth Tables

100000247 and 100000238

Positive logic: AB=X

A	B	Output X*
0	0	0
1	0	0
0	1	0
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000154

Positive logic: $\overline{AB}$=X

A	B	Output X*
0	0	1
1	0	1
0	1	1
1	1	0

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000117

Positive logic: A + B = X

A	B	Output X*
0	0	0
1	0	1
0	1	1
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000228
Truth Table

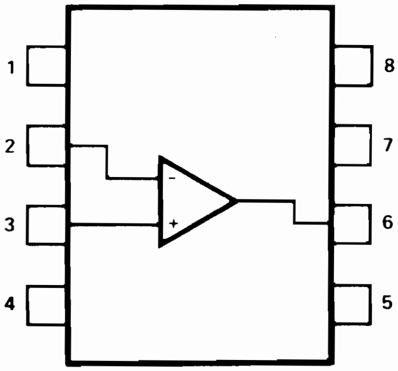
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible.

100000156 100000319

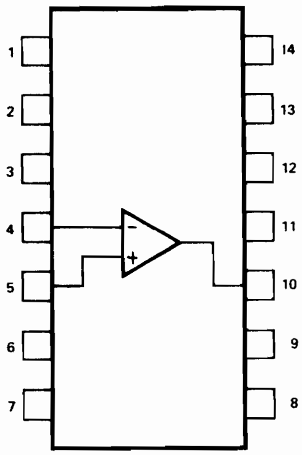
Pin Configuration

100000156



(Top View)

100000319



High Performance Operational Amplifier

Pin Designations

1. Offset Null	5. Offset Null
2. Inv. Input	6. Output
3. Non-Inv. Input	7. V^+
4. V^-	8. NC

This device is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and temperature stability.

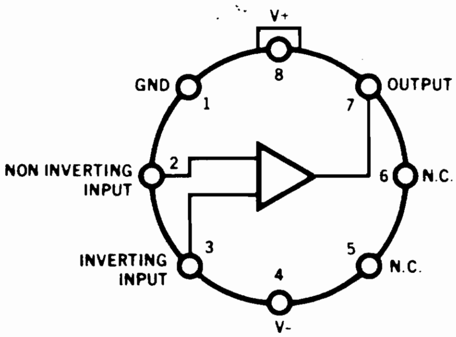
The device is short-circuit protected and allows for nulling of offset voltage.

100000059 100000157 100000324

High-Speed Differential Comparator

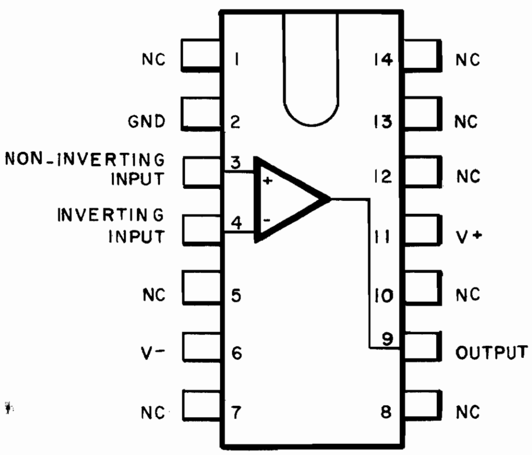
Pin Configurations

100000059, 100000324



Note: Pin 4 connected to case.

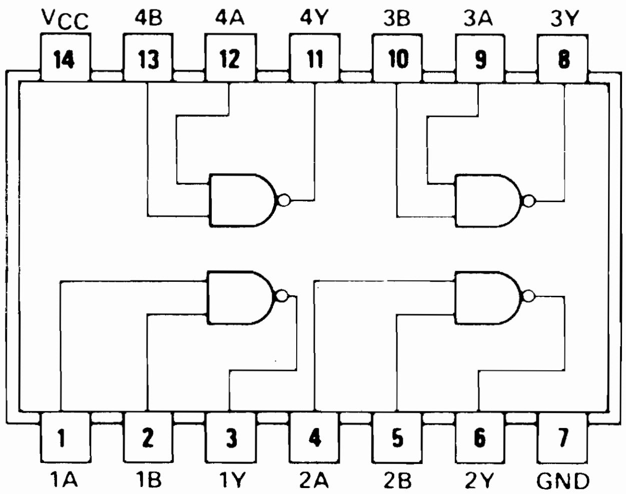
100000157



The 100000059 & 100000324 (can) and 100000157 (DIP) are differential voltage comparators intended for applications requiring high accuracy fast response times. Constructed on a single silicon chip, the devices are useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high-noise immunity line receiver.

100000158 100000340 100000515

Pin Configuration



Quadruple 2-Input Positive-NAND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

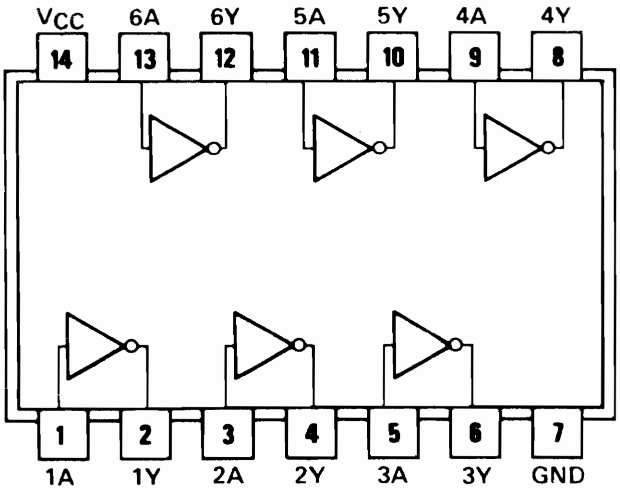
Positive logic: $Y = \overline{AB}$

Note: The 100000158 is a Schottky device.

REV. 03

100000159

Pin Configuration



Hex Inverter

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

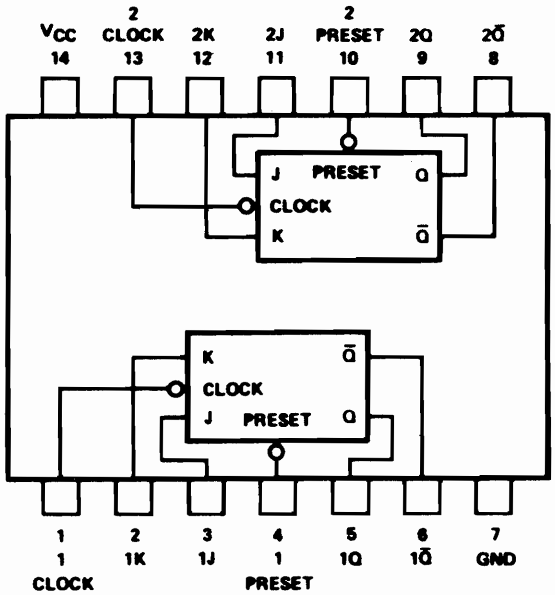
Positive logic: $Y = \overline{A}$

Note: The 100000159 is a Schottky device.

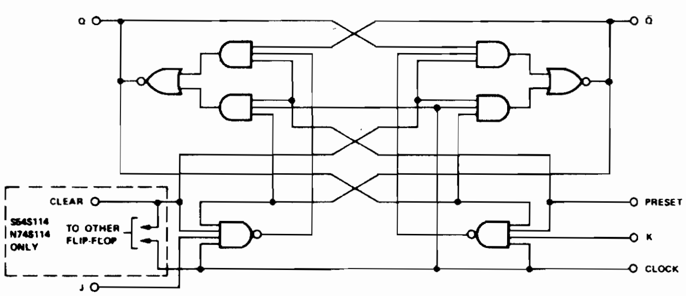
100000160

Dual J-K Edge-Triggered Flip-Flops

Pin Configuration



Logic Diagram (Each Flip-Flop)



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Truth Table

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Notes:

t_n = bit time before clock pulse.

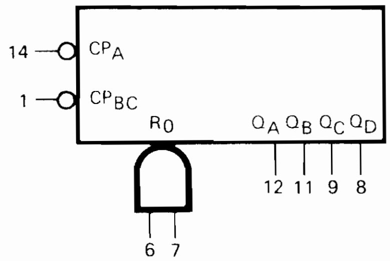
t_{n+1} = bit time after clock pulse.

These monolithic dual flip-flops are designed so that when the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

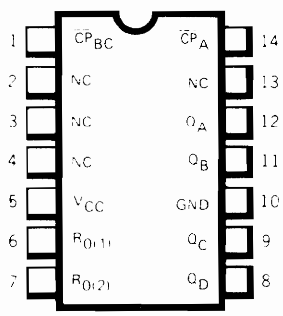
Note: The 100000160 is a Schottky device.

100000161

Logic Symbol

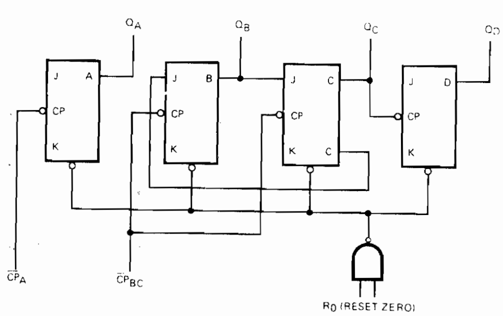


Connection Diagram Dip (Top View)



NC = No internal connection

Logic Diagram



Divide-By-Twelve Counter (Divide-By-Two and Divide-By-Six)

Logic Diagram/Pin Designations

V_{CC} = Pin 5
Gnd = Pin 10
N. C. = Pins 2, 3, 4, 13

Pin Names

R_0 .... Reset-Zero Inputs
$\overline{CP}_A$ .... Clock Input
$\overline{CP}_{BC}$............... Clock Input
Q_A, Q_B, Q_C, Q_D .... Count Outputs

Truth Table

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

Notes:

1. Output Q_A connected to input $\overline{CP}_{BC}$.
2. To reset all outputs to Low level both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at High level state.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a Low level to count.

The 100000161 is a 4-Bit Binary Counter consisting of four master slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A grated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a Low level. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

Continued ....

100000161
(Continued)

A. When used as a divide-by-twelve counter, output Q_A must be externally connected to input $\overline{CP}_{BC}$. The input count pulses are applied to input $\overline{CP}_A$. Simultaneous divisions of 2, 6 and 12 are performed at the Q_A, Q_C and Q_D outputs as shown in the truth table.

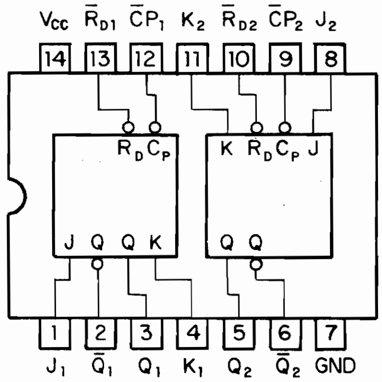
B. When used as a divide-by-six counter, the input count pulses are applied to input $\overline{CP}_{BC}$. Simultaneously, frequency divisions of 3 and 6 are available at the Q_C and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

These circuits are completely compatible with TTL and DTL logic families.

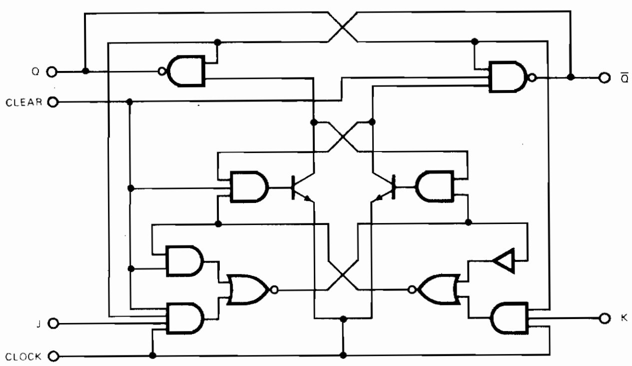
100000162

Dual JK Master/Slave Flip-Flop With Separate Clears and Clocks

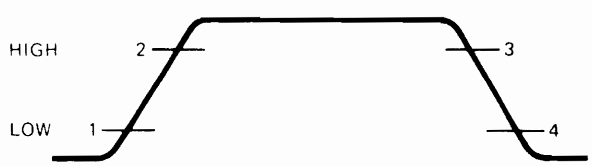
Pin Configuration



Logic Diagram
(Each Flip-Flop)



Clock Waveform



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Positive logic:

LOW input to clear sets Q to LOW level. Clear is independent of clock.

Truth Table

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Notes:

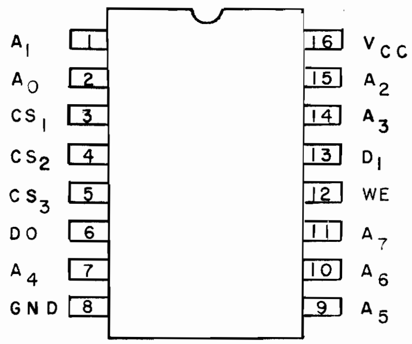
t_n = Bit time before clock pulse.

t_{n+1} = Bit time after clock pulse.

These Dual JK Master/Slave flip-flops have a separate clear and a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; and 4) transfer information from master to slave.

100000164

Pin Configuration



256-Bit Bipolar Random Access Memory

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Memory Function Table

Chip Selects	Write Enable	Operation	Output
All "0"	"0"	Write	Logical "1" State
All "0"	"1"	Read	Complement of data written in memory
One or More "1"	X	Hold	Logical "1" State

The 100000164 integrated circuit is a high speed, fully decoded, static bipolar 256-bit random access memory in a 256x1 organization. This device provides uncommitted collector output and three chip selects.

Operation

Read

The memory is addressed through the A_0-A_7 inputs which select one of the 256 words. The chip is enabled by placing all chip selects (CS) to logic "0". If any or all CS inputs are logic "1", then the device will be disabled. If the write enable (WE) is at logic "1" the stored bit is read out of DO.

Write

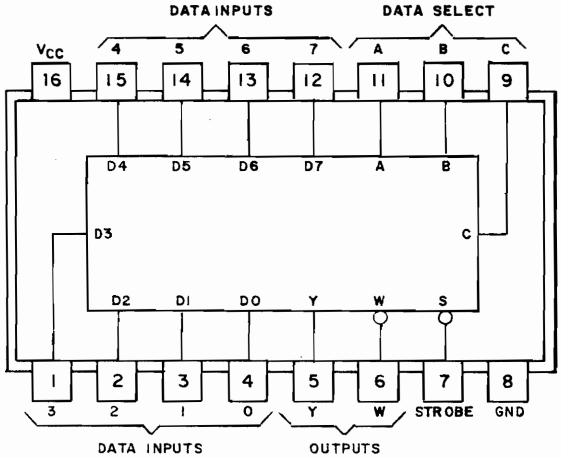
The memory is addressed through the A_0-A_7 inputs which select one of the 256 words. The chip is enabled by placing all the CS inputs to logic "0". If the WE input is at logic "0", the data on terminal DI is written into the addressed word.

When WE returns to logic "1", the information that was written in is now read out; however, each word read out is the complement of what was written in.

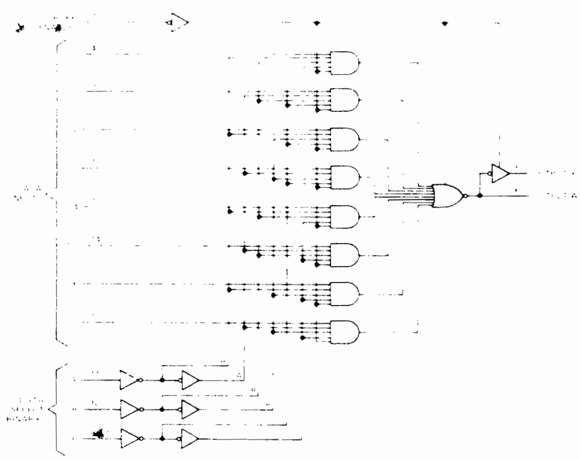
100000165

Data Selector/Multiplexer With 3-State Outputs

Pin Configuration



Logic Diagram



Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Function Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off).
D0, D1 .... D7 = the level of the respective D input.

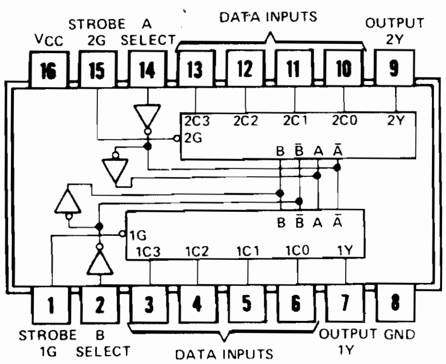
This monolithic data selector/multiplexer contains full on-chip binary decoding to select one-of-eight data sources and a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

Note: The 100000165 is a Schottky device.

100000166

Dual 4-Line-To-1-Line Data Selector - Multiplexer

Pin Configuration



Positive Logic: See Function Table

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

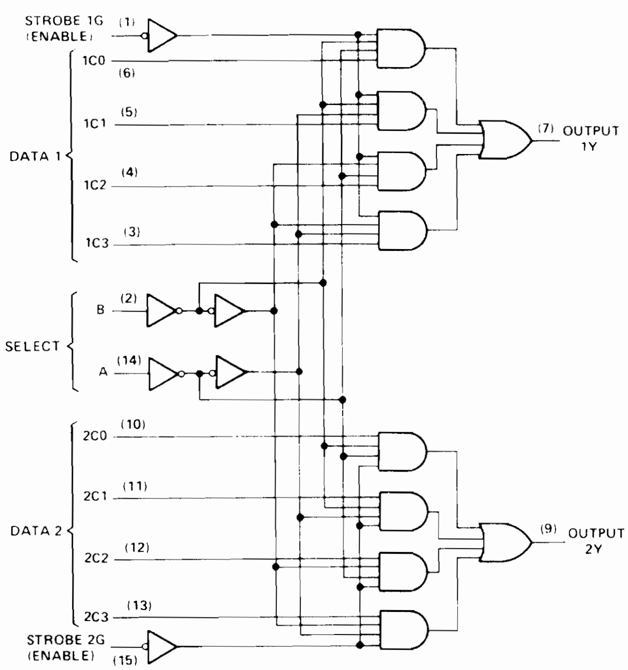
Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select Inputs A and B are common to both sections.

H = high level; L = low level; X = irrelevant.

Logic Diagram



This monolithic, data selector-multiplexer contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates.

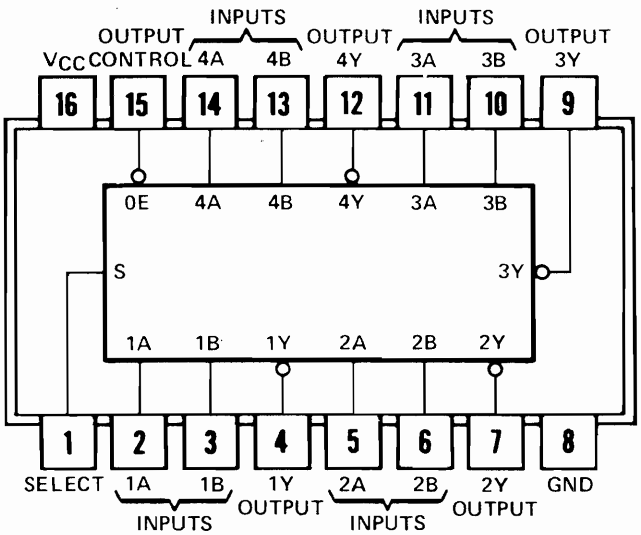
Separate strobe inputs are provided for each of the two four-line sections.

Note: The 100000166 is a Schottky device.

100000167 100000187

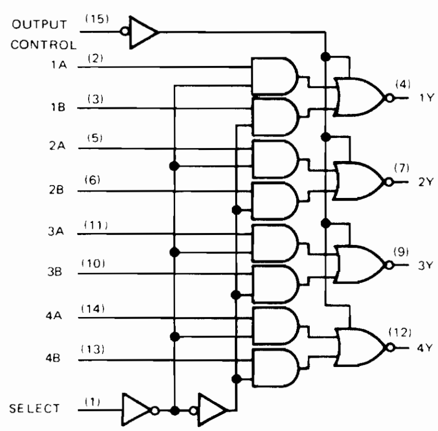
Pin Configuration

100000167/100000187



Logic Diagram

100000167/100000187



Quadruple 2-Line-To-1-Line Data Selectors/Multiplexers

Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Function Table

Inputs			Output Y	
Output Control	Select	A B	'167	'187
H	X	X X	Z	Z
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

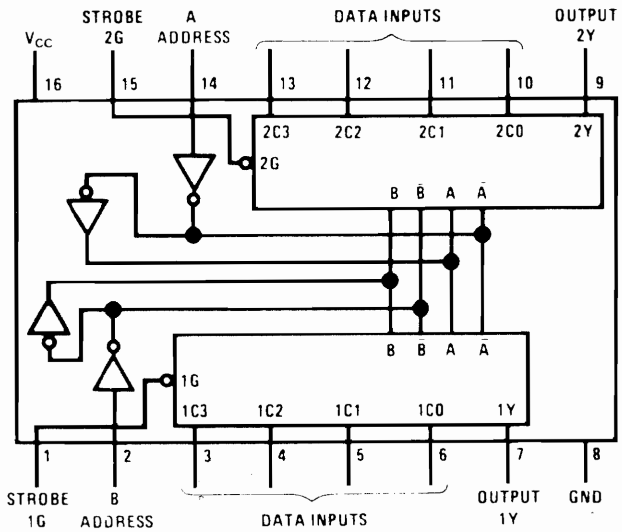
H = high level, L = low level, X = irrelevant.
Z = high impedance (off).

These Schottky-clamped multiplexers have three-state outputs which can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

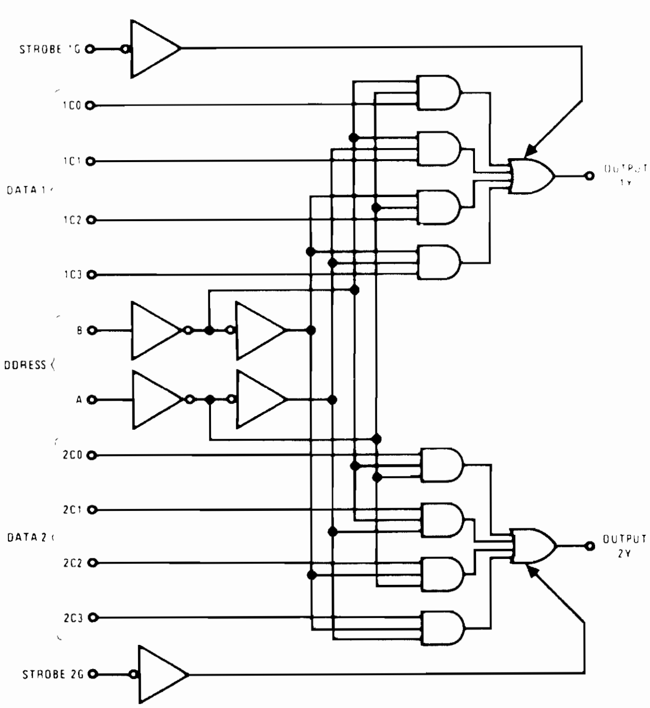
This three-state output means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

100000168

Pin Configuration



Logic Diagram



Dual 4-Line-To-1-Line Multiplexer

Logic Diagram/Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Truth Table

Address Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	Hi-Z
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

X = Don't care.

This device acts as a double-pole four-throw switch. One data line is selected from each of two four-line inputs. Two select lines determine which of the four inputs is chosen; however, the same input of both four-line selections will be selected. The logic allows outputs of the device to be tied to outputs of similar devices and connected to a common bus-line. Nominal TTL outputs cannot be connected due to the low-impedance logical "1" output current which one device would have to sink from the other. If, however, on all but one of the connected devices both the upper and lower output transistors are turned off, then the one remaining device in the normal low-impedance state will have to supply to or sink from the other devices only a small amount of leakage current. The strobe input is used to place the output in the high-impedance state.

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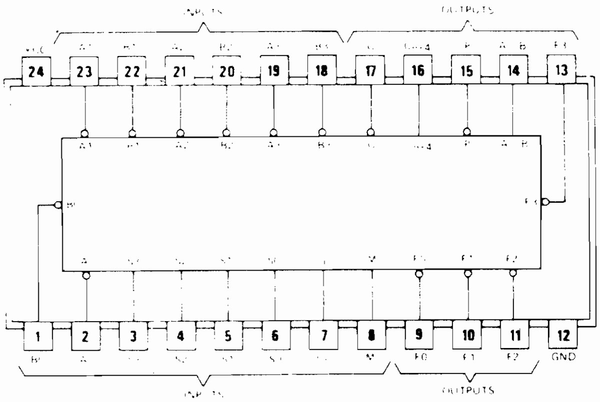
Arithmetic Logic Units/Function Generators

Pin Configuration



Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A=B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
Gnd	12	Ground

These arithmetic logic units (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip, and perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with 100000100 or 100000170, full carry look-ahead circuits, high-speed arithmetic operations can be performed. If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay is minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These devices will accommodate active-high or active-low data if the pin designations are interpreted as follows:

Continued.....

100000084 100000169 100000306

Continued

Table 1

Selection S3 S2 S1 S0	M = H Logic Functions	Active-High Data M = L: Arithmetic Operations C_n = H (no carry)	C_n = L (with carry)
L L L L	$F = \overline{A}$	F = A *	F = A Plus 1
L L L H	$F = \overline{A + B}$	F = A + B	F = (A + B) Plus 1
L L H L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ Plus 1
L L H H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L H L L	$F = \overline{AB}$	$F = A$ Plus $A\overline{B}$	$F = A$ Plus $A\overline{B}$ Plus 1
L H L H	$F = \overline{B}$	$F = (A + B)$ Plus $A\overline{B}$	$F = (A + B)$ Plus $A\overline{B}$ Plus 1
L H H L	$F = A \oplus B$	F = A Minus B Minus 1	F = A Minus B
L H H H	$F = A\overline{B}$	$F = A\overline{B}$ Minus 1	$F = A\overline{B}$
H L L L	$F = \overline{A} + B$	F = A Plus AB	F = A Plus AB Plus 1
H L L H	$F = \overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	$F = (A + \overline{B})$ Plus AB	$F = (A + \overline{B})$ Plus AB Plus 1
H L H H	F = AB	F = AB Minus 1	F = AB
H H L L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H H L H	$F = A + \overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H H H L	F = A + B	$F = (A + \overline{B})$ Plus A	$F = (A + \overline{B})$ Plus A Plus 1
H H H H	F = A	F = A Minus 1	F = A

* Each bit is shifted to the next more significant position.

Table 2

Selection S3 S2 S1 S0	M = H Logic Functions	Active-Low Data M = L: Arithmetic Operations C_n = L (no carry)	C_n = H (with carry)
L L L L	$F = \overline{A}$	F = A Minus 1	F = A
L L L H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L L H L	$F = \overline{A} + B$	$F = A\overline{B}$ Minus 1	$F = A\overline{B}$
L L H H	F = 1	F = Minus 1 (2's Comp)	F = Zero
L H L L	$F = \overline{A + B}$	$F = A$ Plus $(A + \overline{B})$	$F = A$ Plus $(A + \overline{B})$ Plus 1
L H L H	$F = \overline{B}$	$F = AB$ Plus $(A + \overline{B})$	$F = AB$ Plus $(A + \overline{B})$ Plus 1
L H H L	$F = \overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L H H H	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ Plus 1
H L L L	$F = \overline{A}B$	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H L L H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	$F = A\overline{B}$ Plus (A + B)	$F = A\overline{B}$ Plus (A + B) Plus 1
H L H H	F = A + B	F = A + B	F = (A + B) Plus 1
H H L L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H H L H	$F = A\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H H H L	F = AB	$F = A\overline{B}$ Plus A	$F = A\overline{B}$ Plus A Plus 1
H H H H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.

Pin No.	Active-high data Table 1	Active-low data Table 2
2	A_0	$\overline{A}_0$
1	B_0	$\overline{B}_0$
23	A_1	$\overline{A}_1$
22	B_1	$\overline{B}_1$
21	A_2	$\overline{A}_2$
20	B_2	$\overline{B}_2$
19	A_3	$\overline{A}_3$
18	B_3	$\overline{B}_3$
9	F_0	$\overline{F}_0$
10	F_1	$\overline{F}_1$
11	F_2	$\overline{F}_2$
13	F_3	$\overline{F}_3$
7	$\overline{C}_n$	C_n
16	$\overline{C}_{n+4}$	C_{n+4}
15	X	$\overline{P}$
17	Y	$\overline{G}$

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

These devices can also be utilized as comparators. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

Input C_n	Output C_{n+4}	(Figure 1) Active-high Data	(Figure 2) Active-low Data
H	H	$A \leqslant B$	$A \geqslant B$
H	L	$A > B$	$A < B$
L	H	$A < B$	$A > B$
L	L	$A \geqslant B$	$A \leqslant B$

Continued....

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Continued

Figure 1

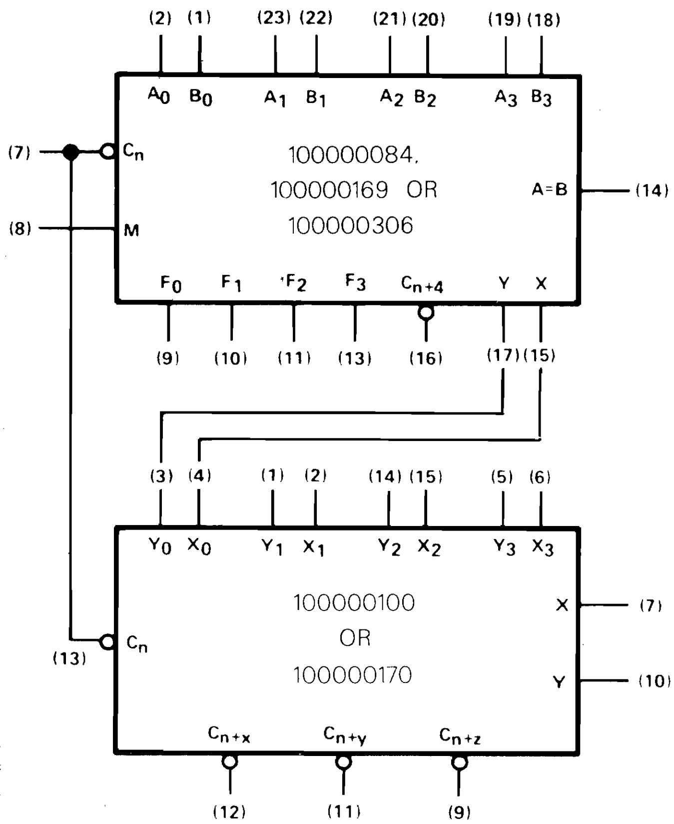
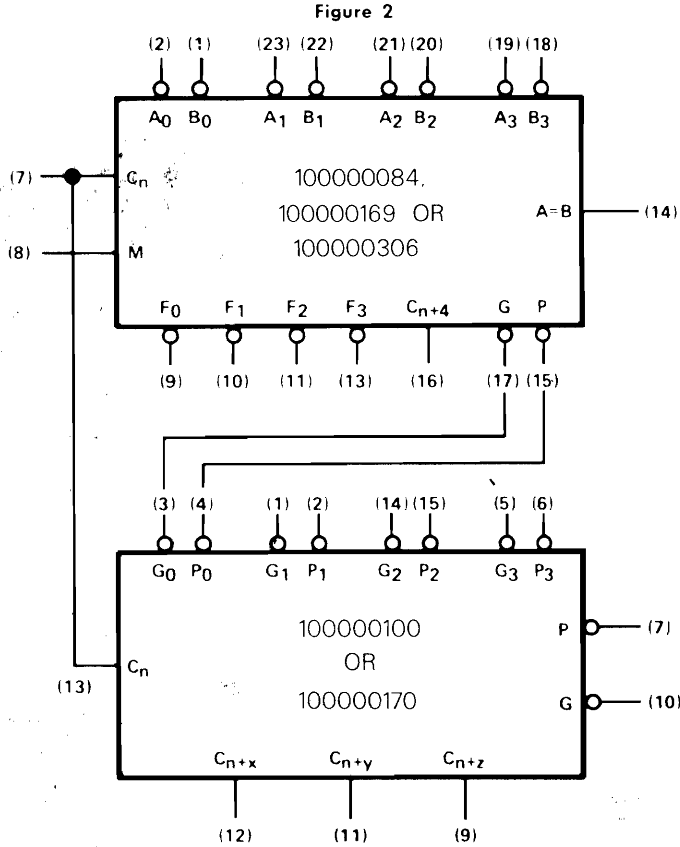


Figure 2



These circuits have been designed to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR and OR functions.

ALU Signal Designations

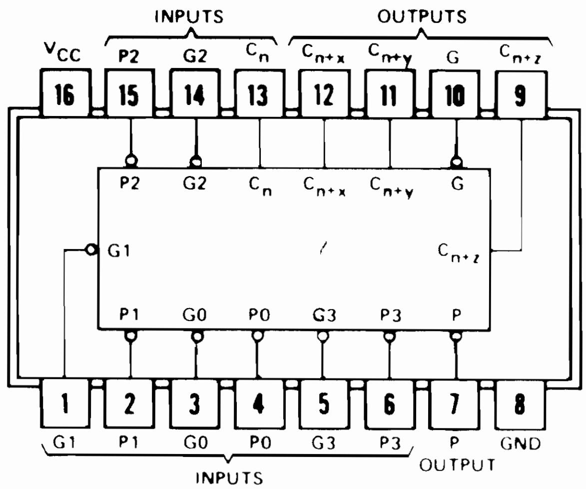
These devices can be used with the signal designations of either Figure 1 or Figure 2. The logic functions and arithmetic operations obtained with the signal designations of Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

Note: The 100000169 is a Schottky device.

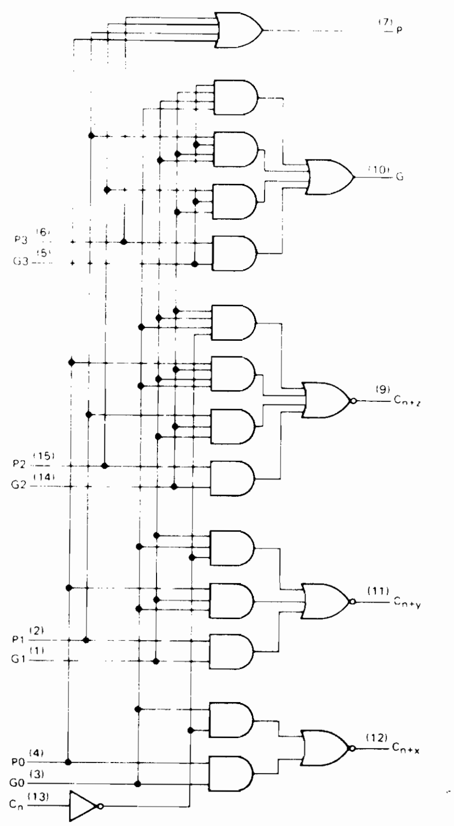
100000100 100000170

Look-Ahead Carry Generators

Pin Configuration



Logic Diagram



Pin Designations

Designation	Pin Nos.	Function
G0, G1, G2, G3	3, 1, 14, 5	Active-Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active-Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active-Low Carry Generate Output
P	7	Active-Low Carry Propagate Output
V_{CC}	16	Supply Voltage
Gnd	8	Ground

Positive Logic:

$$C_{n+x} = \overline{G}_0 + \overline{P}_0 C_n$$

$$C_{n+y} = \overline{G}_1 + \overline{P}_1\overline{G}_0 + \overline{P}_1\overline{P}_0 C_n$$

$$C_{n+z} = \overline{G}_2 + \overline{P}_2\overline{G}_1 + \overline{P}_2\overline{P}_1\overline{G}_0 + \overline{P}_2\overline{P}_1\overline{P}_0 C_n$$

$$\overline{G} = \overline{G}_3(\overline{P}_3+\overline{G}_2)(\overline{P}_3+\overline{P}_2+\overline{G}_1)(\overline{P}_3+\overline{P}_2+\overline{P}_1+\overline{G}_0)$$

$$\overline{P} = \overline{P}_3\overline{P}_2\overline{P}_1\overline{P}_0$$

These devices are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry and propagate-carry functions are provided as enumerated in the pin designation table above.

When used in conjunction with arithmetic logic units, 100000084 or 100000169, these generators provide high-speed carry look-ahead capability for any word length.

Carry input and output of the 100000084 or 100000169 are in their true form and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU.

Note: The 100000170 is a Schottky device.

100000171

Pin Configuration

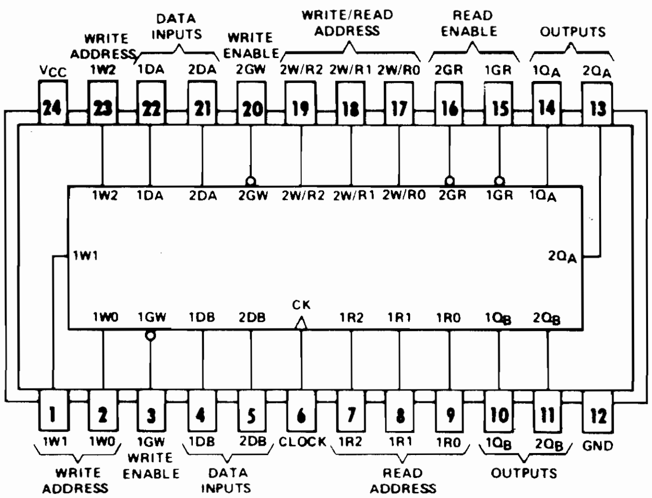
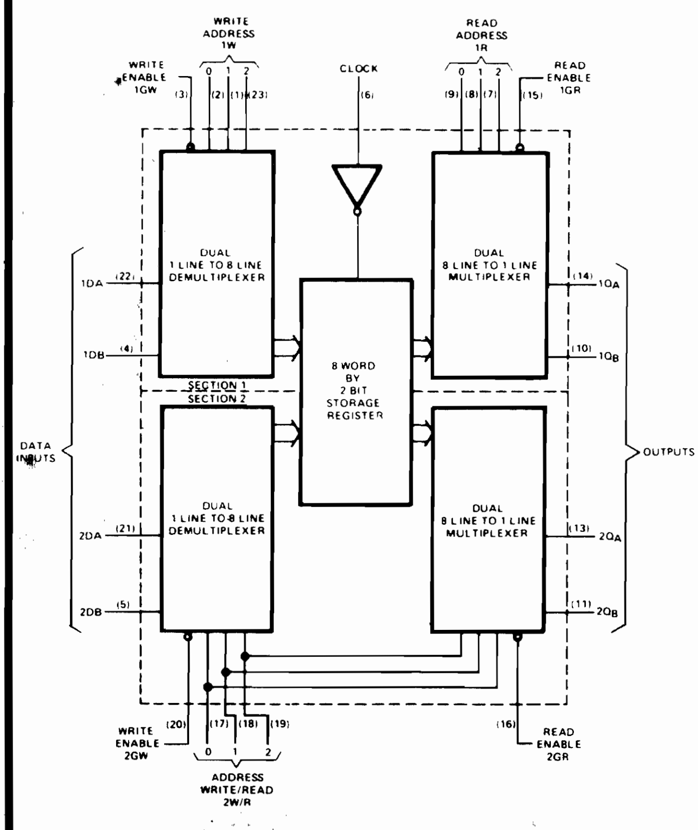


Figure A



16-Bit Multiple-Port Register File With 3-State Outputs

Pin Designations

V_{CC} = Pin 24

Gnd = Pin 12

The 100000171 is a high-performance 16-bit register file organized as eight words of two bits each.

Multiple address decoding circuitry is used so that the read and write operation can be performed independently on two word locations. This provides a true simultaneous read/write capability. Basically, the file consists of two distinct sections (see Figure A).

Section 1 permits the writing of data into any two-bit word location while reading two bits of data from another location simultaneously. To provide this flexibility, independent decoding is incorporated.

Section 2 of the register file is similar to section 1 with the exception that common read/write address circuitry is employed. This means that section 2 can be utilized in one of three modes:

1) Writing new data into two bits.
2) Reading from two bits.
3) Writing into and simultaneously reading from the same two bits.

Regardless of the mode, the operation of section 2 is entirely independent of section 1.

The three-state outputs of this register file permit connection of up to 129 compatible outputs to a common system bus. The outputs are controlled by the read-enable circuitry so that they operate as standard TTL totem-pole outputs when the appropriate read-enable input is low or they are placed in a high-impedance state when the associated read-enable input is at a high logic level.

Functions of the inputs and outputs are as shown in the following table:

Continued ....

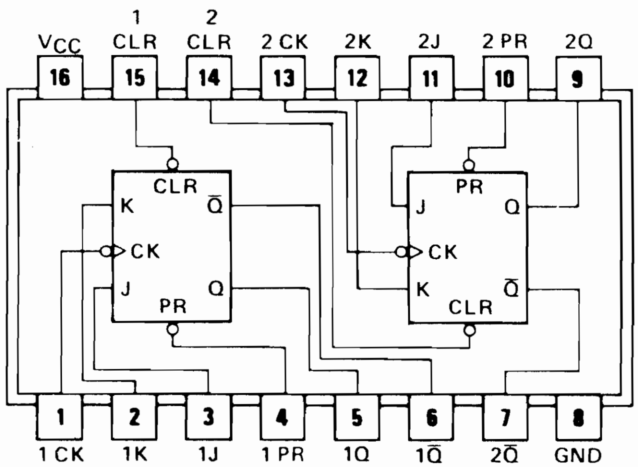
100000171

Continued

Function	Section 1	Section 2	Description
Write Address	1W0, 1W1, 1W2	2W/R0, 2W/R1, 2W/R2	Binary write address selects one of eight two-bit word locations.
Write Enable	1GW	2GW	When low, permits the writing of new data into the selected word location on a positive transition of the clock input.
Data Inputs	1DA, 1DB	2DA, 2DB	Data at these inputs is entered on a positive transition of the clock input into the location selected by the write address inputs if the write enable input is low. Since the two sections are independent, it is possible for both write functions to be activated with both write addresses selecting the same word location. If this occurs and the information at the data inputs is not the same for both sections (i.e., 1DA $\neq$ 2DA and/or 1DB $\neq$ 2DB) the low-level data will predominate in each bit and be stored.
Read Address	1R0, 1R1, 1R2	Common with write address	Binary write address selects one of eight two-bit word locations.
Read Enable	1GR	2GR	When read enable is low, the outputs assume the levels of the data stored in the location selected by read address inputs. When read enable is high, the associated outputs remain in the high-impedance state and neither significantly load nor drive the lines to which they are connected.
Data Outputs	$1Q_A$, $1Q_B$	$2Q_A$, $2Q_B$	
Clock	CK		The positive-going transition of the clock input will enter new data into the addressed location if the write enable input is low. The clock is common to both sections.

100000172

Pin Configuration



Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

Logic Diagram/Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Function Table

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

Notes:

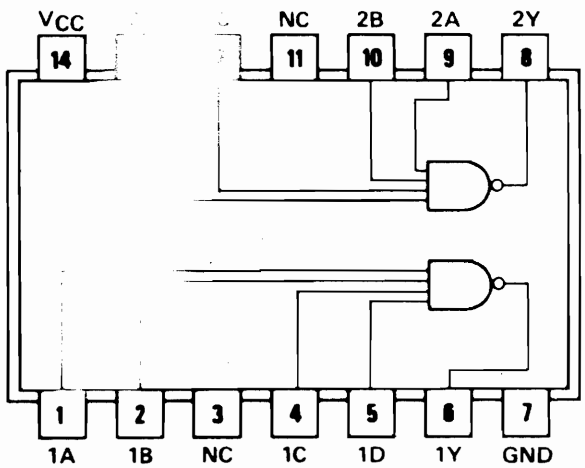
H = high level (steady state).
L = low level (steady state).
X = irrelevant.
↓ = transition from high to low level.
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE = Each output changes to the complement of its previous level on each active transition of the clock.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Note: The 100000172 is a Schottky device.

REV. 03

100000173

Configuration



Dual 4-Input Positive-NAND 50 Ohm Line Driver

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

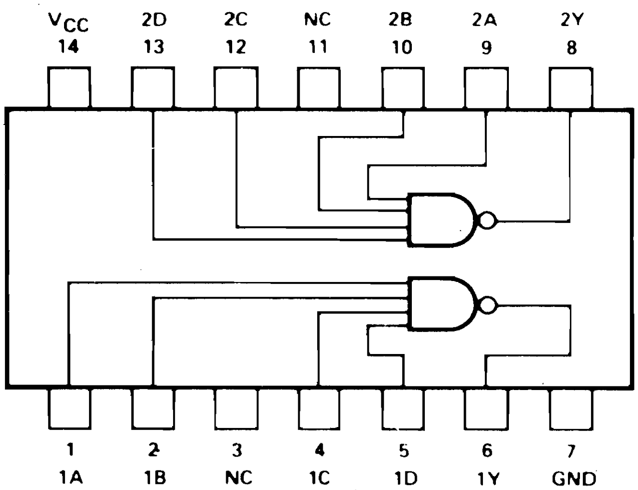
NC = No internal connection

Positive logic: $Y = \overline{ABCD}$

Note: The 100000173 is a Schottky device.

100000174

Pin Configuration



Positive-NAND Gate With Open-Collector Outputs

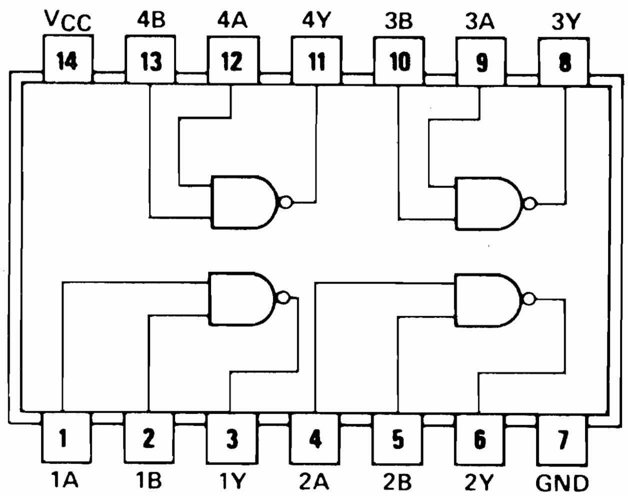
Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Note: The 100000174 is a Schottky device.

100000175

Pin Configuration



Quadruple 2-Input Positive-NAND Gate With Open-Collector Outputs

Logic Diagram/Pin Designations

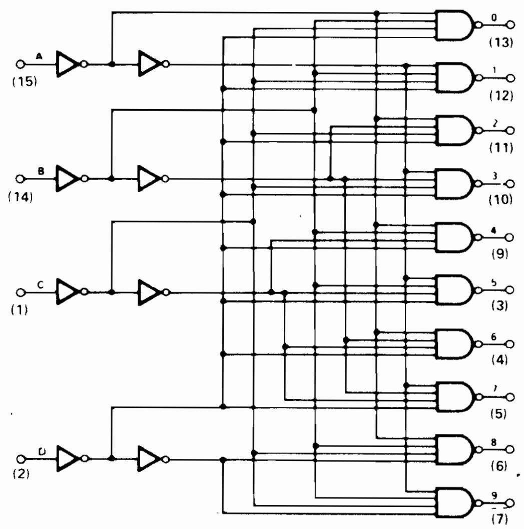
V_{CC} = Pin 14
Gnd = Pin 7

Positive logic: $Y = \overline{AB}$

Note: The 100000175 is a Schottky device.

100000178

Logic Diagram



BCD-To-Decimal Decoder

Logic Diagram/Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Truth Table

Input State				Output States									
A	B	C	D	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

The 100000178 is a gate array for decoding and logic conversion.

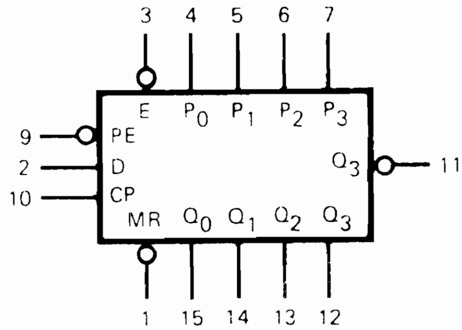
This device converts a 4-line input code (with 1-2-4-8 weighting) to a one-of-ten output, as shown in the Truth Table.

Note: The 100000178 is a Schottky device.

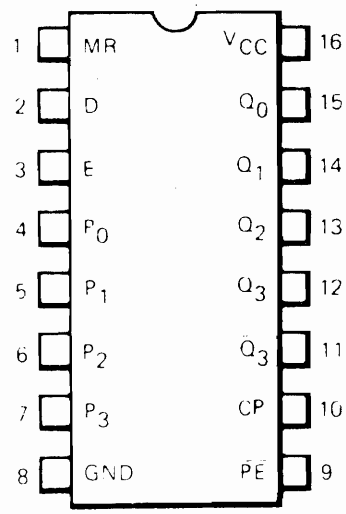
100000180

High Speed 4-Bit Shift Register With Enable

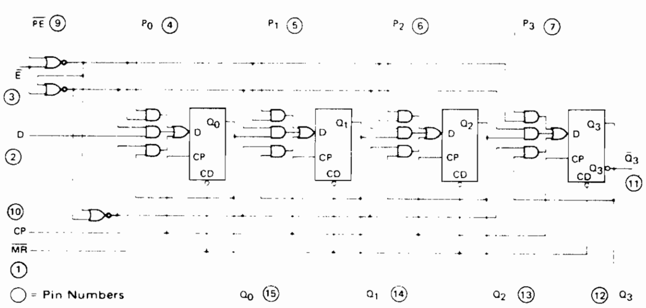
Logic Symbol



Pin Configuration



Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names

$\overline{E}$ .... Active LOW Enable Input
$\overline{PE}$ .... Active LOW Parallel Enable Input
P_0, P_1, P_2, P_3 .. Parallel Data Inputs
CP .... Clock Input
$\overline{MR}$ .... Active LOW Master Reset Input
Q_0 to Q_3 .... Parallel Outputs
$\overline{Q_3}$ .... Last Stage Complementary Output
D .... Serial Data Input

The 100000180 High Speed 4-Bit Shift Register is a multifunctional sequential logic block which is useful in a wide variety of register applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data transfers.

This device has three synchronous modes of operation: shift, parallel load and hold (do nothing). The hold capability permits information storage in the register independent of the clock.

The register is fully synchronous with any output change occurring after the rising clock edge. It features edge triggered type characteristics on all inputs (except $\overline{MR}$), which means there are no restrictions on the activity of these inputs ($\overline{PE}$, $\overline{E}$, P_0, P_1, P_2, P_3, D) for logic operation except for the set up requirements prior to the LOW to HIGH clock transition.

The mode of operation is determined by the two inputs, parallel enable ($\overline{PE}$) and enable ($\overline{E}$), as shown in Table 1. The active LOW enable when HIGH places the register in the hold mode with the register flip-flops retaining their information. When the enable is activated (LOW) the parallel enable ($\overline{PE}$) determines whether the register operates in a shift or parallel data entry mode.

When the enable is LOW and the parallel enable input is LOW, the parallel inputs are selected and will determine the next condition of the register synchronously with the clock as shown in Table 2. In this mode the element appears as four common clocked D flip-flops. With $\overline{E}$ LOW and the $\overline{PE}$

Continued....

input HIGH the device acts as a 4-bit shift register with serial data entry through the D input shown in Table 3. In both cases the next state of the flip-flops occurs after the LOW to HIGH transition of the clock input.

The asynchronous active LOW master reset overrides all inputs and clears the register forcing outputs Q_{0-3} LOW and $\overline{Q}_3$ HIGH.

To provide for left shift operation, P3 is used as the serial data input and Q_0 is the serial data output. The other outputs are tied back to the previous parallel inputs, with Q_3 tied to P_2, Q_2 tied to P_1 and Q_1 tied to P_0.

Table 1
Mode Selection

Mode		$\overline{MR}$	$\overline{E}$	$\overline{PE}$	P_0 P_1 P_2 P_3	D
Synchronous	Parallel Load	H	L	L	Parallel Data Entry	X
	Serial Shift	H	L	H	X X X X	Serial Data Entry
	Hold	H	H	L	X X X X	X
	Hold	H	H	H	X X X X	X
Asynchronous	Reset	L	X	X	All Outputs set LOW	

Table 2
Parallel Data Entry

P_0, P_1, P_2 or P_3 Input at t_n	Q at t_{n+1}
L	L
H	H

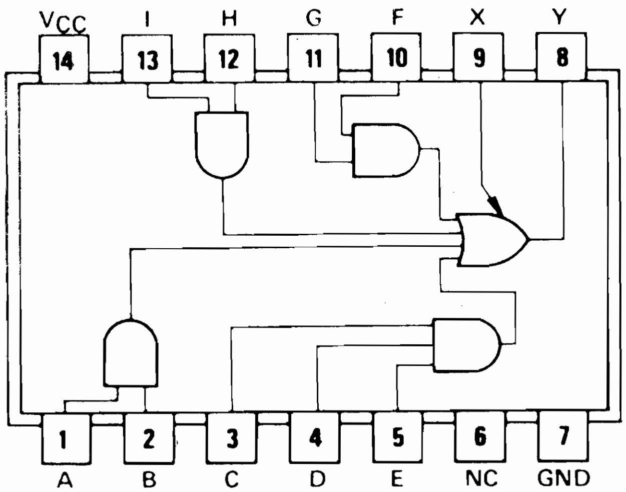
Table 3
Serial Data Entry

D Input at t_n	Q_0 at t_{n+1}
L	L
H	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
t_n = Present State
t_n+1 = State after Next Clock

100000181

Pin Configuration



Expandable 4-Wide AND-OR Gates

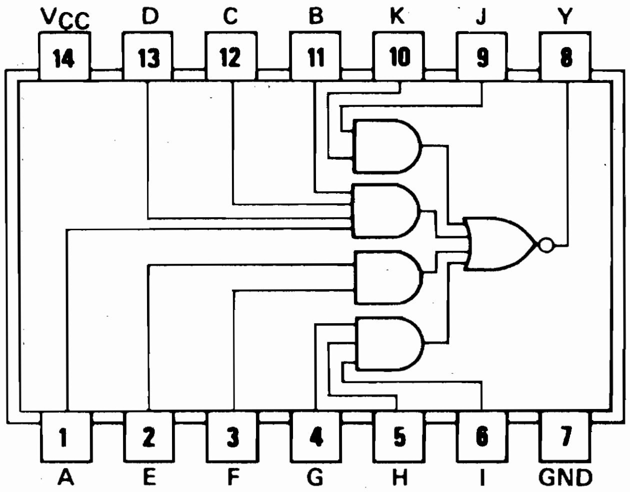
Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Positive logic: Y = AB+CDE+FG+HI+X

100000182

Pin Configuration



4-2-3-2-Input AND-OR-INVERT Gates

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

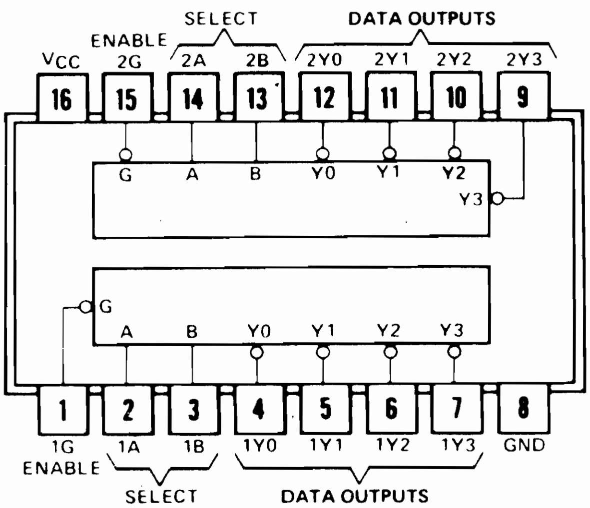
Positive logic: $Y = \overline{ABCD+EF+GHI+JK}$

Note: The 100000182 is a Schottky device.

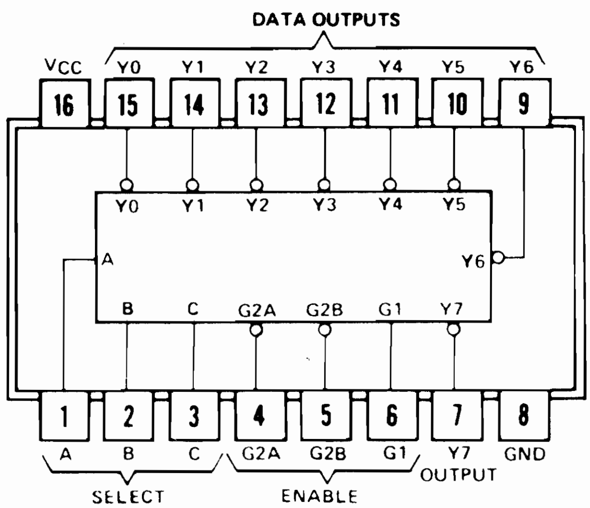
100000185 100000223

Pin Configurations

100000185



100000223



Decoders-Demultiplexers

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Function Table - 100000223

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level; L = low level; X = irrelevant

Function Table - 100000185
(Each Decoder/Demultiplexer)

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level; L = low level; X = irrelevant

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

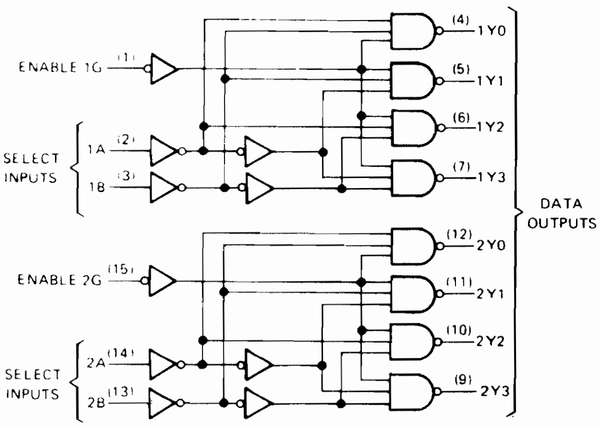
Continued. . . .

100000185 100000223

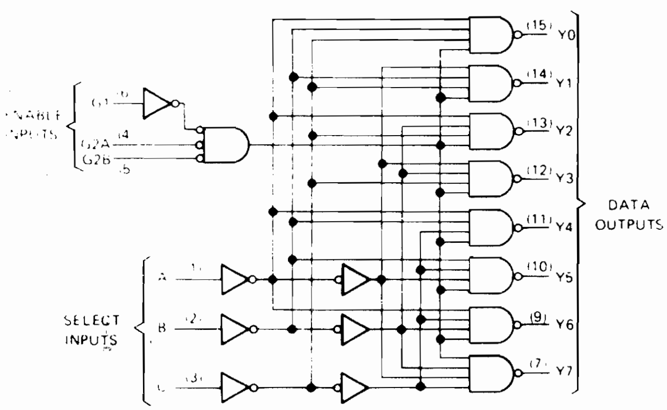
Continued

Logic Diagrams

100000185



100000223



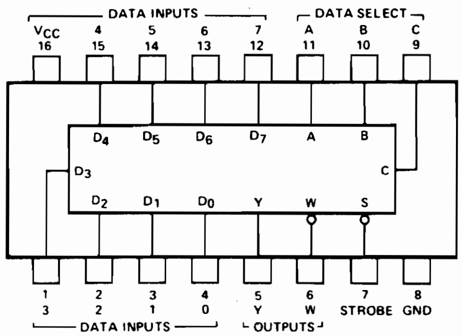
The 100000223 decodes one-of-eight lines, depending on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 100000185 is comprised of two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

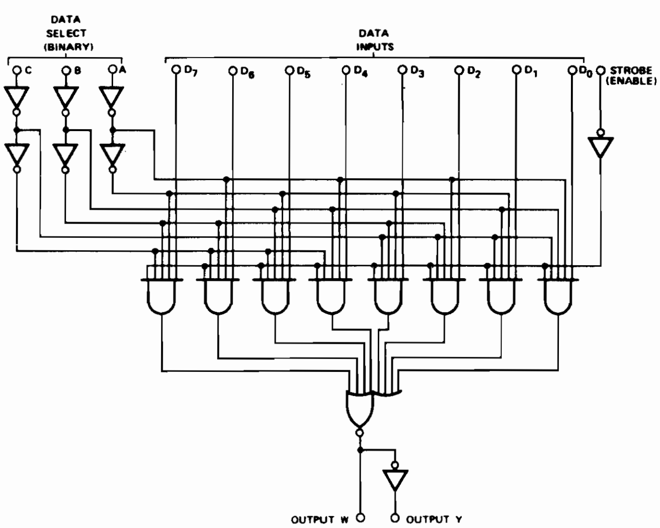
100000186

8-Line-to-1-Line Data Selector/Multiplexer

Pin Configuration



Logic Symbol



Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Truth Table

Inputs											Outputs	
C	B	A	Strobe	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

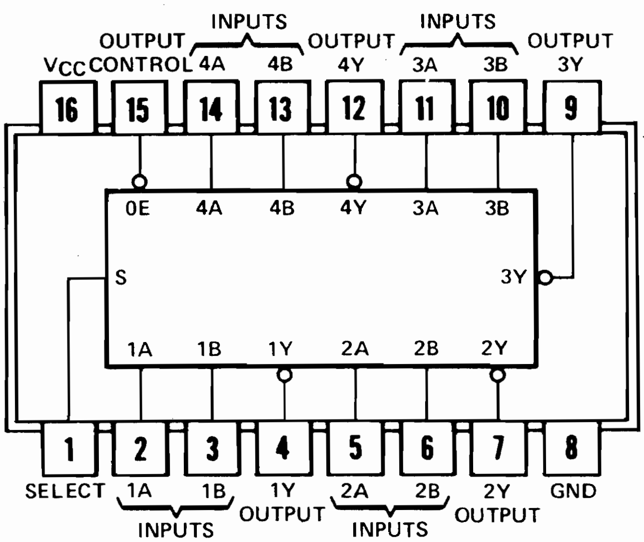
Note: When used to indicate an input, X = irrelevant.

The 100000186 is a one-of-eight data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line.

100000167 100000187

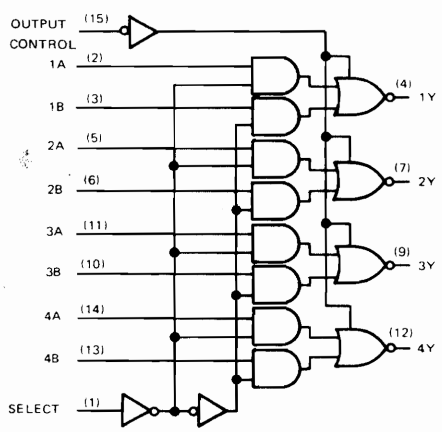
Pin Configuration

100000167/100000187



Logic Diagram

100000167/100000187



Quadruple 2-Line-To-1-Line Data Selectors/Multiplexers

Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Function Table

Inputs			Output Y	
Output Control	Select	A B	'167	'187
H	X	X X	Z	Z
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

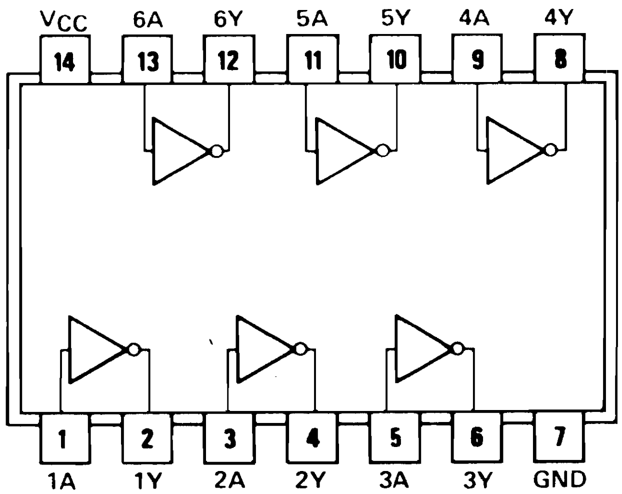
H = high level, L = low level, X = irrelevant,
Z = high impedance (off).

These Schottky-clamped multiplexers have three-state outputs which can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

This three-state output means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

100000188 100000284

Pin Configuration



Hex Inverter With Open-Collector Outputs

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Positive logic: $Y = \overline{A}$

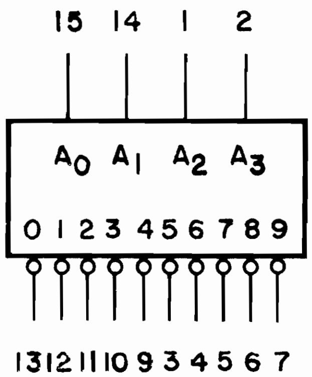
Note: The 100000188 is a Schottky device.

REV. 03

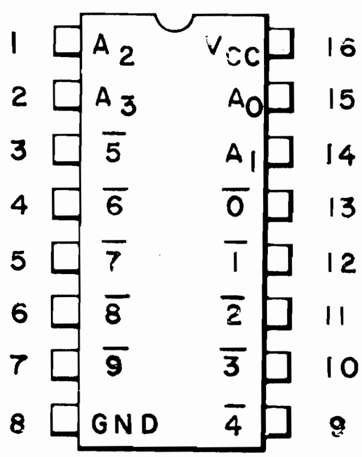
100000189

One-Of-Ten Decoder With Open Collector Output

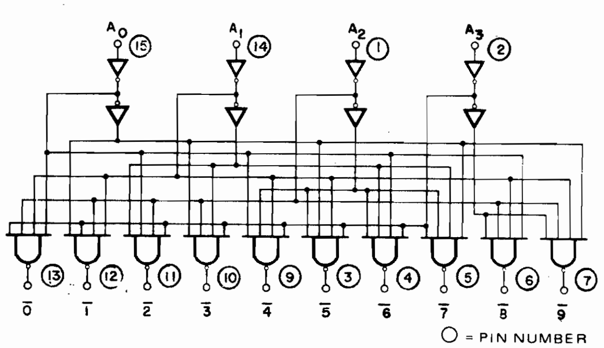
Logic Symbol



Pin Configuration



Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Pin Names

A_0, A_1, A_2, A_3 = Address Inputs
$\overline{0}$ to $\overline{9}$ = Outputs, Active LOW*

* An external pull-up resistor is needed to provide HIGH level drive capability.

Truth Table

A0	A1	A2	A3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

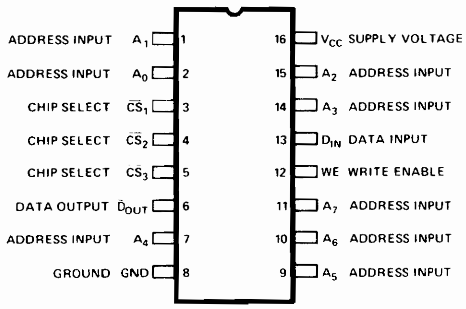
The 100000189 is a multipurpose decoder which accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs. The open collector outputs provide summing of input terms. This device provides the capability in one package to generate and sum any or all of the minterms of three variables, or the first 10-of-16 minterms of four variables.

The logic design ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

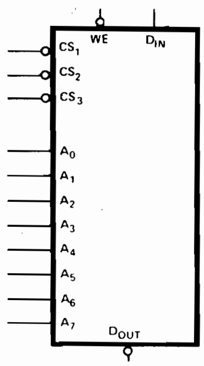
100000190

High Speed Fully Decoded 256-Bit RAM

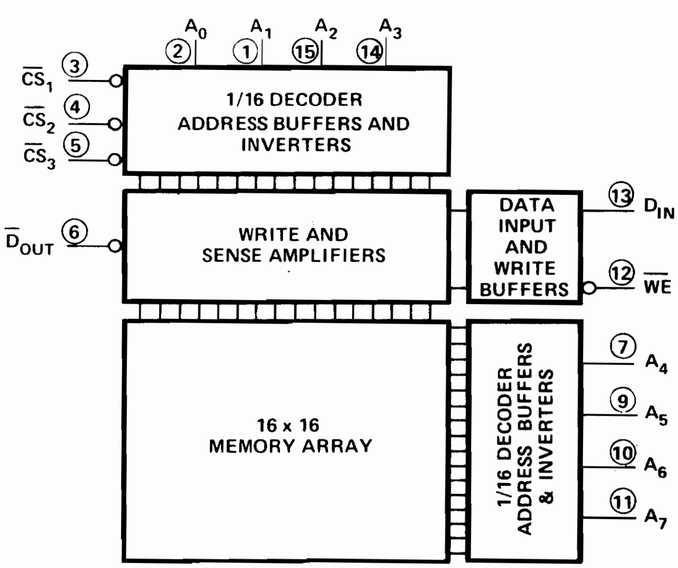
Pin Configuration



Logic Symbol



Functional Block Diagram



Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Pin Names:

D_{IN}	Data Input
A_0-A_7	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}_1$-$\overline{CS}_3$	Chip Select
$\overline{D}_{OUT}$	Data Output

Truth Table

Chip Select	Write Enable	Operation	Output
All Low	Low	Write	Complement of data input
All Low	High	Read	Complement of written data
One or more High	Don't Care	Hold	High Impedance State

The 100000190 is a high speed, fully decoded, 256 bit read/write random access memory. The device features three chip-select inputs and a three-state output.

100000191

High Speed Fully Decoded 1024-Bit Read Only Memory

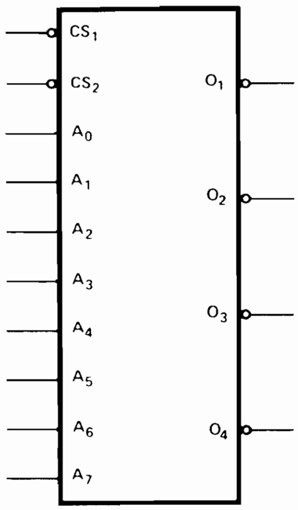
Pin Designations

V_{CC} = Pin 16

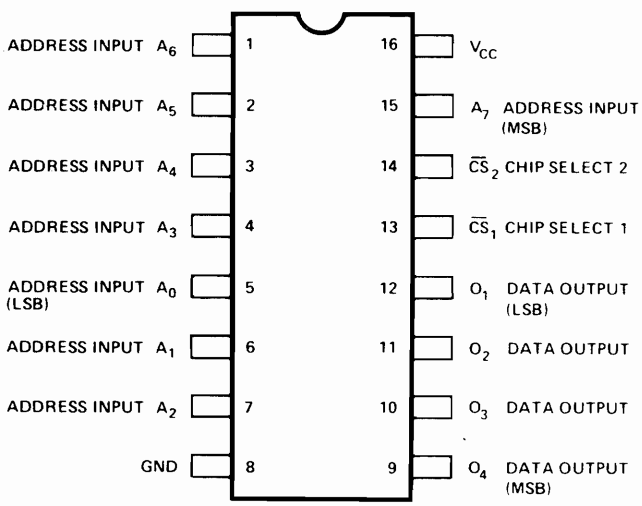
Gnd = Pin 8

The 100000191 is a fully decoded 1024-bit read only memory organized as 256 words by 4 bits.

Logic Symbol

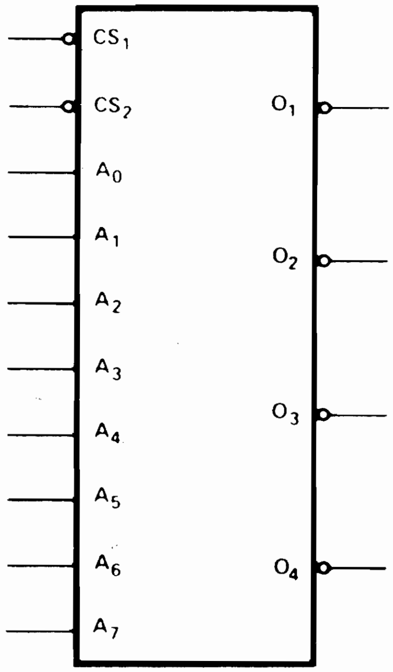


Pin Configuration

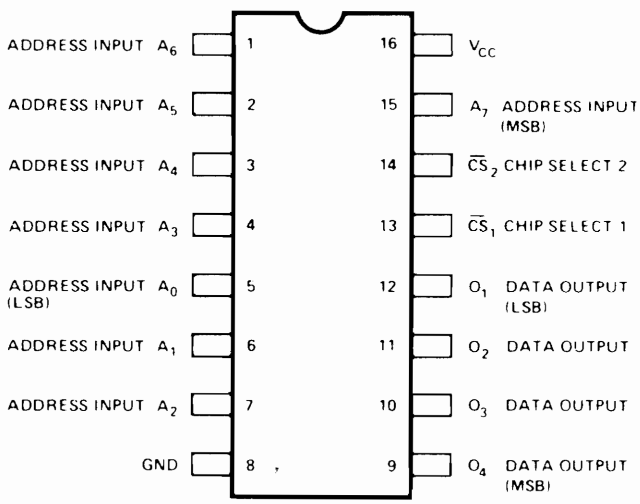


100000192

Logic Symbol



Pin Configuration



High Speed Electrically Programmable 1024-Bit Read Only Memory

Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

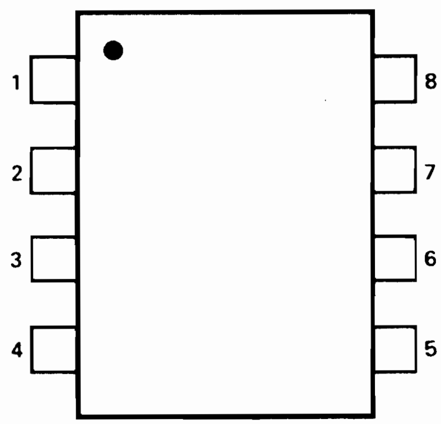
The 100000192 is a 1024-bit (256 word by 4 bit) electrically programmable ROM. All outputs are low; logic output high levels can be electrically programmed in selected bit locations.

The same address inputs are used for both programming and reading.

100000193

Timer

Pin Configuration



Pin Designations

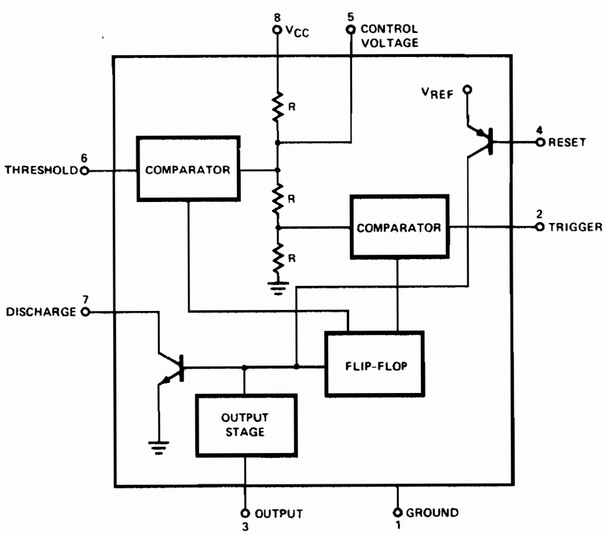
1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

The 100000193 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. Additional terminals are provided for triggering or re-setting, if desired.

In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. For a stable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor.

The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

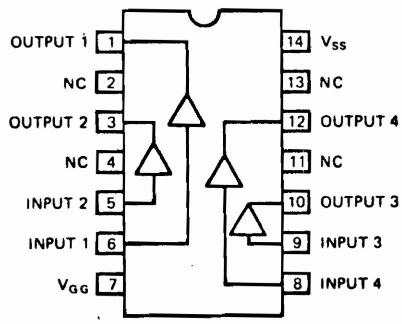
Functional Block Diagram



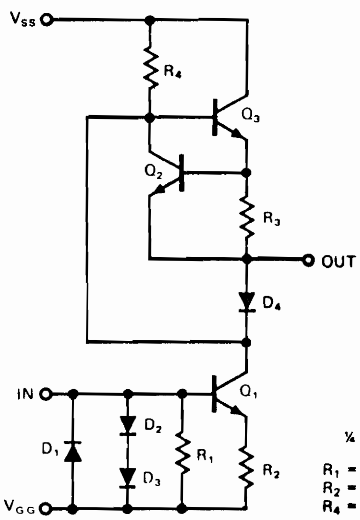
100000194

Quad MOS Clock Driver

Pin Configuration



Schematic Diagram



¼ IM5003

$R_1 = 300\Omega$
$R_2 = R_3 = 1.6\Omega$
$R_4 = 1K\Omega$

Logic Diagram/Pin Designations

V_{SS} = Pin 14

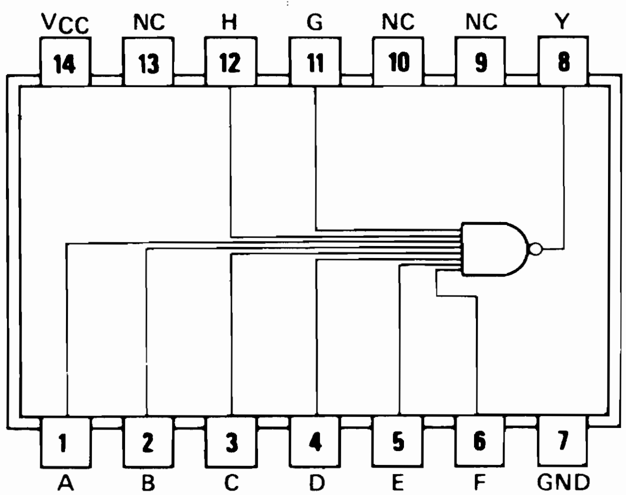
V_{GG} = Pin 7

The 100000194 is a monolithic quad driver designed primarily for use as a ı MOS clock driver. It can be driven by high current TTL buffers or drivers, either directly or through input coupling capacitors, if level shifting is required.

REV. 03

100000195 100000337

Pin Configuration



8-Input Positive-NAND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

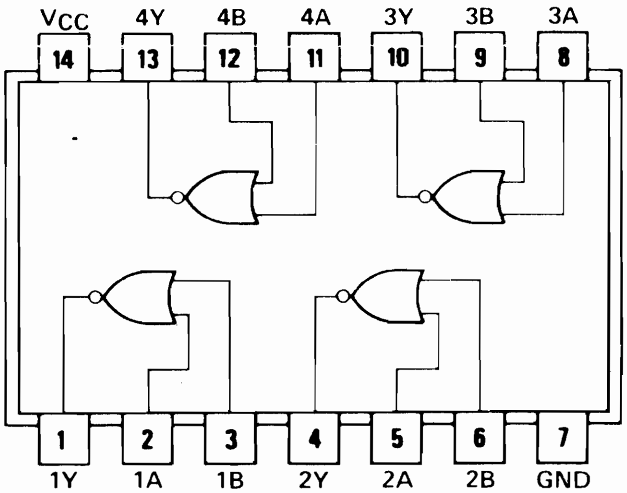
NC = No internal connection

Positive logic: $Y = \overline{ABCDEFGH}$

REV. 03

100000196

Pin Configuration



Quadruple 2-Input Positive-NOR Buffers With Open-Collector Outputs

Logic Diagram/Pin Designations

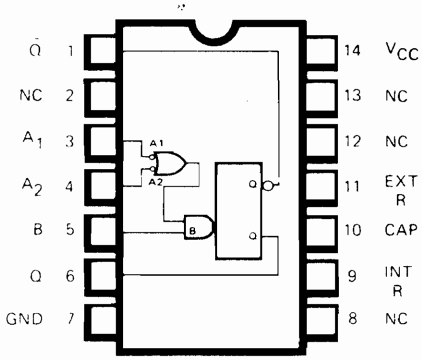
V_{CC} = Pin 14

Gnd = Pin 7

Positive logic: $Y = \overline{A+B}$

100000197

Pin Configuration



Monostable Multivibrator

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Truth Table

t_n Input			t_{n+1} Input			Output
A_1	A_2	B	A_1	A_2	B	
H	H	L	H	H	H	Inhibit
L	X	H	L	X	L	Inhibit
X	L	H	X	L	L	Inhibit
L	X	L	L	X	H	One Shot
X	L	L	X	L	H	One Shot
H	H	H	X	L	H	One Shot
H	H	H	L	X	H	One Shot
X	L	L	X	H	L	Inhibit
L	X	L	H	X	L	Inhibit
X	L	H	H	H	H	Inhibit
L	X	H	H	H	H	Inhibit
H	H	L	X	L	L	Inhibit
H	H	L	L	X	L	Inhibit

$H = V_{IH} \geq 2V$

$L = V_{IL} \leq 0.8V$

Notes:

1. t_n = time before input transition.
2. t_{n+1} = time after input transition.
3. X indicates that either a High or Low may be present.
4. NC = No internal connection.
5. A_1 and A_2 are negative edge triggered-logic inputs and will trigger the one shot when either or both go to Low level with B at High level.
6. B is a positive Schmitt-trigger input for slow edges or level detection and will trigger the one shot when B goes to High level with either A_1 or A_2 at Low level. (See Truth Table.)
7. External timing capacitor may be connected between pin 10 (positive) and pin 11. With no external capacitance, an output pulse width of typically 30ns is obtained.
8. To use the internal timing resistor (2kΩ nominal), connect pin 9 to pin 14.
9. To obtain variable pulse width, connect external variable resistance between pin 9 and pin 14. No external current limiting is needed.
10. For accurate repeatable pulse widths, connect an external resistor between pin 11 and pin 14 with pin 9 open-circuit.

Continued....

100000197
Continued

The 100000197 is a TTL Monostable Multivibrator with dc triggering from positive or gated negative going inputs and with inhibit facility. Both positive and negative going output pulses are provided with full fan out to 10 normalized loads.

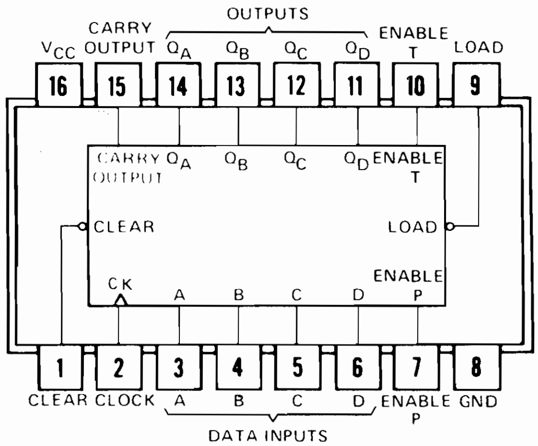
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1.0 V/s, providing the circuit with noise immunity of typically 1.2V. A high immunity to V_{CC} noise of typically 1.5V is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40ns to 40s by choosing appropriate timing components. With no external timing components (i.e., pin 9 connected to pin 14, pins 10, 11 open) an output pulse of typically 30ns is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

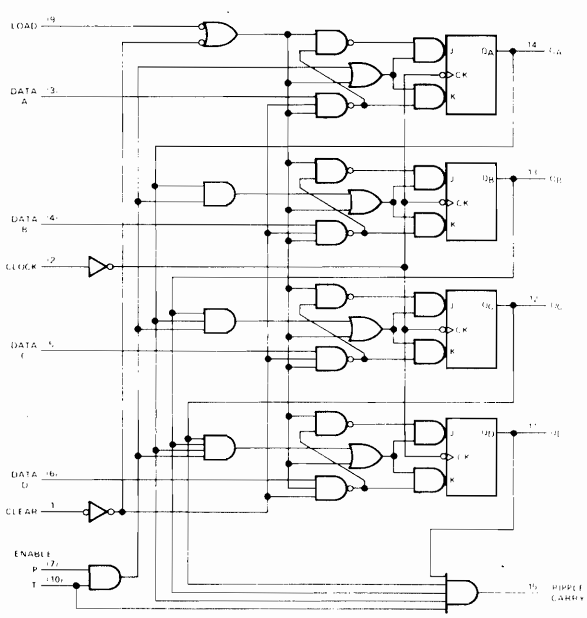
Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 40kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T, R_T \log_e 2$. Duty cycles as high as 90% are achieved when using R_T = 40kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

100000198

Pin Configuration



Logic Diagram



Synchronous 4-Bit Counter

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

This synchronous, presettable 4-bit binary counter features an internal carry look-ahead for application in high-speed counting schemes.

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000(LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output. This positive overflow carry pulse can be used to enable successive cascaded stages. High-to-low transitions at the enable P or T inputs should occur only when the clock input is high.

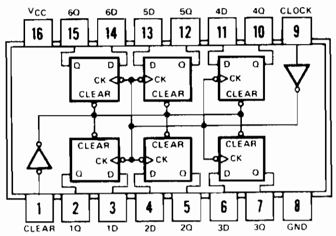
100000199 100000200 100000204 100000205

Hex-Quadruple D-Type Flip-Flops with Clear

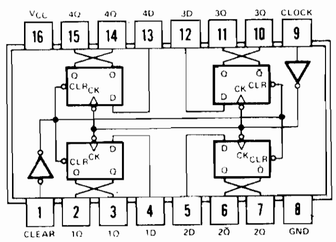
Note: 100000199 and 100000204 - Hex
100000200 and 100000205 - Quadruple

Pin Configurations

100000199/100000204



100000200/100000205



Pin Designations

100000199 and 100000204

V_{CC} = Pin 16
Gnd = Pin 8

100000200 and 100000205

V_{CC} = Pin 16
Gnd = Pin 8

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

Notes:

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.
* = Type 100000200 and 100000205 only.

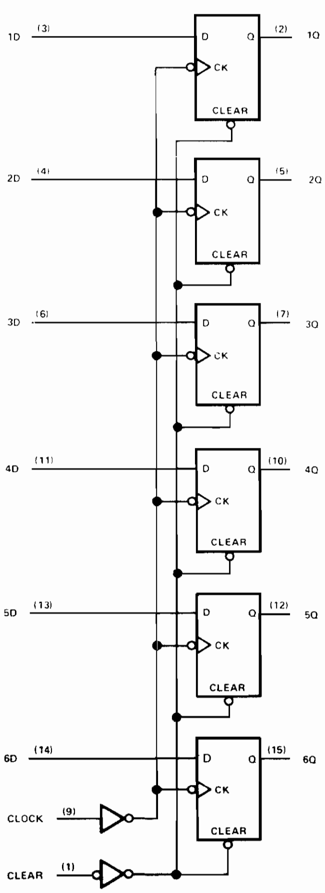
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the Quadruple devices feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

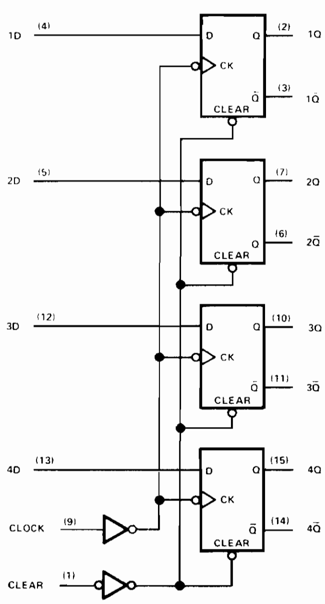
Note: The 100000204 and 100000205 are Schottky devices.

Functional Block Diagrams

100000199/100000204



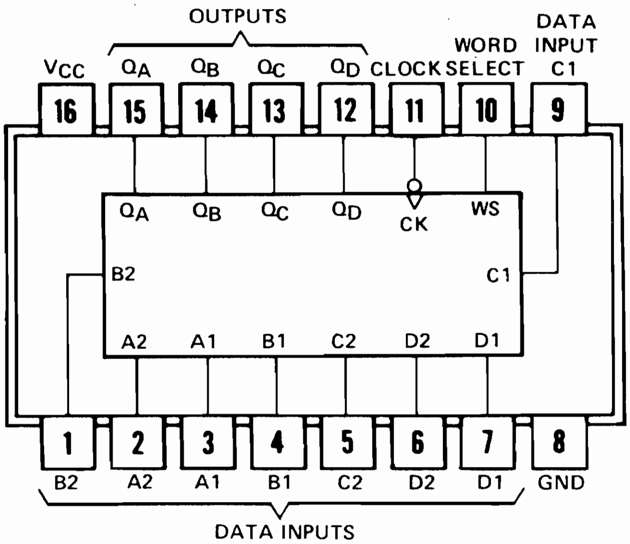
100000200/100000205



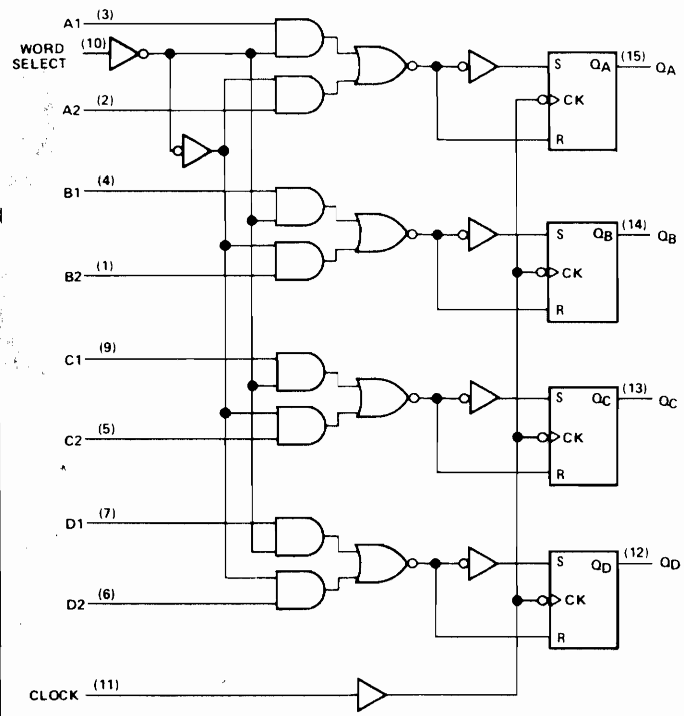
 . . . dynamic input activated by transition from a high level to a low level.

100000201

Pin Configuration



Logic Diagram



. . Dynamic input activated by a transition from a high level to a low level

Quadruple 2-Input Multiplexer With Storage

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Function Table

Inputs		Outputs			
Word Select	Clock	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

Notes:

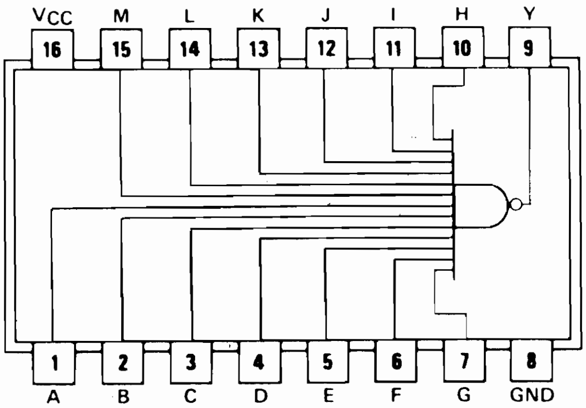
H = high level (steady state).
L = low level (steady state).
X = irrelevant (any input, including transitions).
 = transition from high to low level.
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc., entered on the most recent ↓ transition of the clock input.

This monolithic quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions (100000240 and 100000200) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

100000203

Pin Configuration



13-Input Positive-NAND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

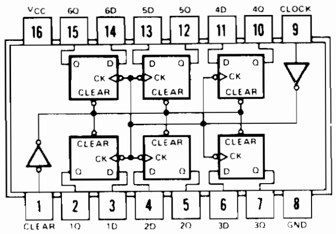
Positive logic: Y = $\overline{ABCDEFGHIJKLM}$

Note: The 100000203 is a Schottky device.

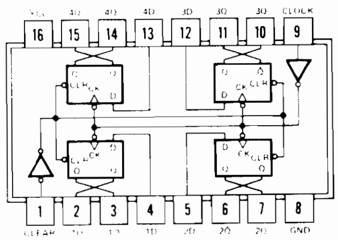
100000199 100000200
100000204 100000205

Pin Configurations

100000199/100000204

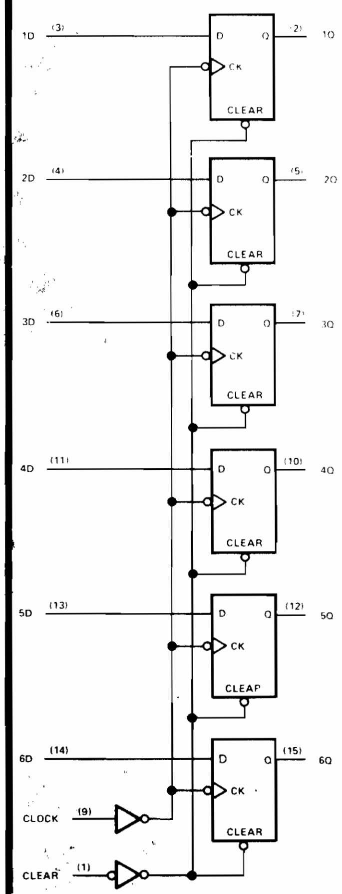


100000200/100000205

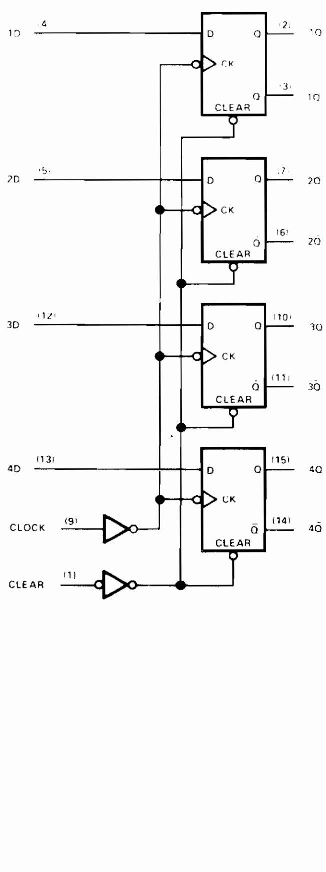


Functional Block Diagrams

100000199/100000204



100000200/100000205



dynamic input activated by transition from a high level to a low level

Hex-Quadruple D-Type Flip-Flops with Clear

Note: 100000199 and 100000204 - Hex
100000200 and 100000205 - Quadruple

Pin Designations

100000199 and 100000204

V_{CC} = Pin 16
Gnd = Pin 8

100000200 and 100000205

V_{CC} = Pin 16
Gnd = Pin 8

Function Table
(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

Notes:

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.
* = Type 100000200 and 100000205 only.

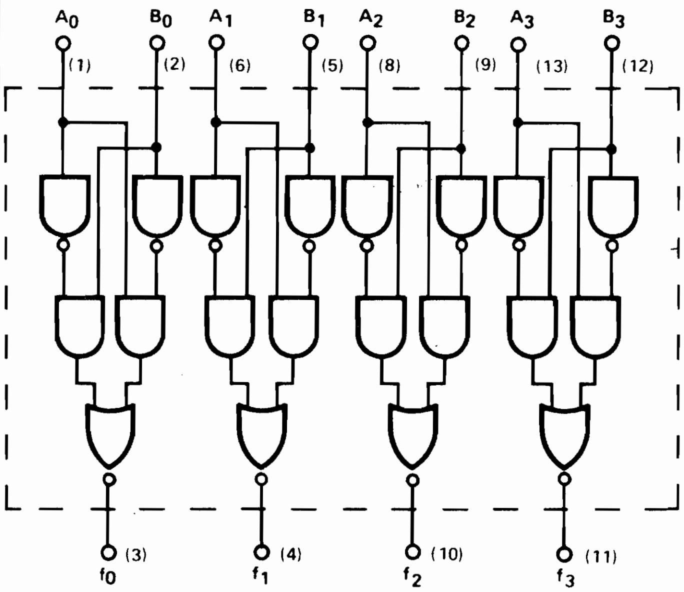
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the Quadruple devices feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Note: The 100000204 and 100000205 are Schottky devices.

100000206

Logic Diagram



4-Bit Quad Exclusive-NOR

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

A	B	f
0	0	1
1	0	0
0	1	0
1	1	1

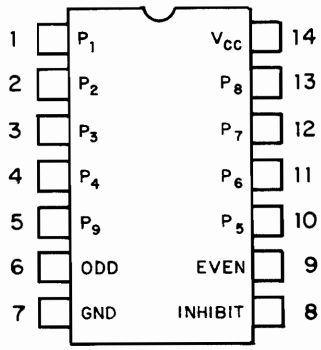
The 100000206 contains four independent Exclusive-NOR gates which may be used to implement digital comparison functions. The device outputs are open collector to facilitate implementation of multiple-bit comparisons; a 4-bit comparison is made by connecting the outputs of the four independent gates together.

Note: The 100000206 is a Schottky device.

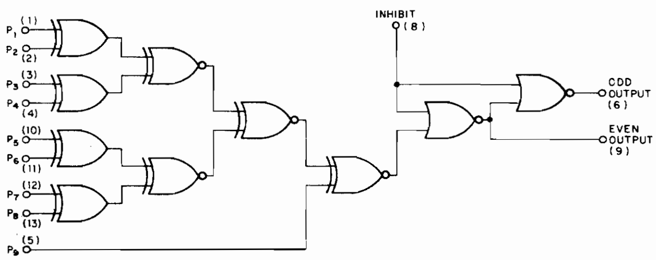
REV. 03

100000207

Pin Configuration



Logic Diagram



( )=Denotes Pin Number

9-Bit Parity Generator and Checker

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Logic Equations:

Odd =

$$P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$$

Even =

$$\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$$

The 100000207 9-Input Parity Generator/Parity Checker is an ultra high speed Schottky MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided. An INHIBIT input is provided to disable both outputs of the device. (A logic 1 on the INHIBIT input forces both outputs to a logic 0).

When used as a Parity Generator, the 100000207 supplies a parity bit which is transmitted together with the data word.

At the receiving end, the device acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

100000208

256-Bit Bipolar Programmable ROM (32 × 8 PROM)

Logic Diagram/Pin Designations

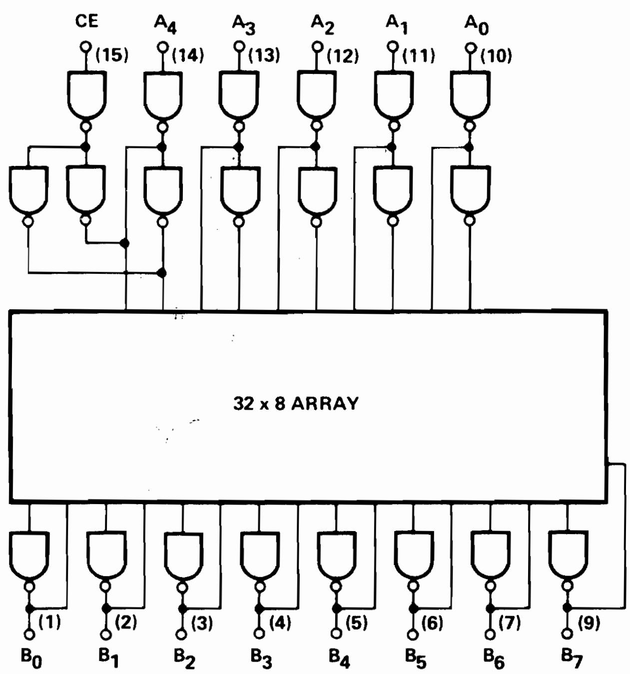
V_{CC} = Pin 16

Gnd = Pin 8

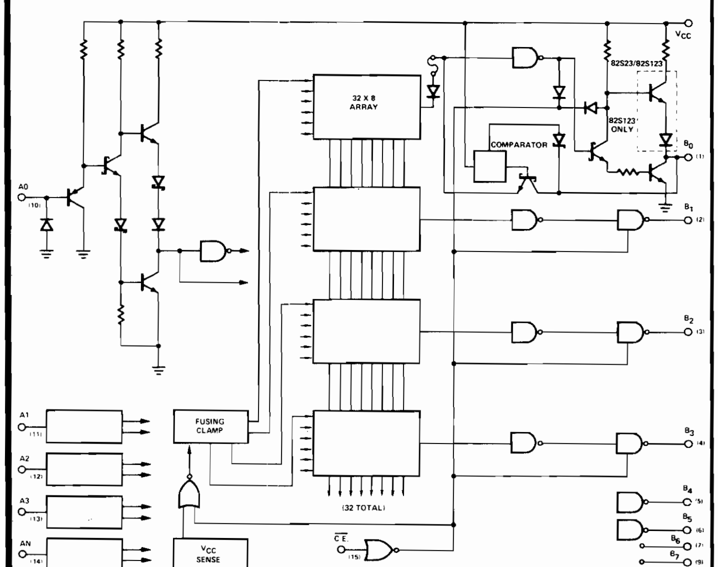
The 100000208 is a Bipolar 256-Bit Read Only Memory organized as 32 words by 8 bits per word. A chip enable line is provided, and the outputs are Tristate to allow for memory expansion capability.

Note: The 100000208 is a Schottky device.

Logic Diagram



Functional Block Diagram



100000211

16-Bit Associative-Content Addressable Memory

Logic Diagram/Pin Designations

V_{CC} = Pin 24

Gnd = Pin 12

The 100000211 is a high speed 16-bit associative random access memory. It is a linear select 4-word by 4-bit array which performs the equality search on all bits in parallel.

With the bit enable lines $(\overline{E}_0 - \overline{E}_3)$ LOW, the outputs $(M_0 - M_3)$ go HIGH if associated stored data matches the descriptor bits $(\overline{D}_0 - \overline{D}_3)$. If a bit enable line is held HIGH, a match is forced on the corresponding bit in all the words regardless of the state of the descriptor bit $(\overline{D}_0 - \overline{D}_3)$. An inverter is connected to the match output M_0 to give its negation $\overline{M}_0$.

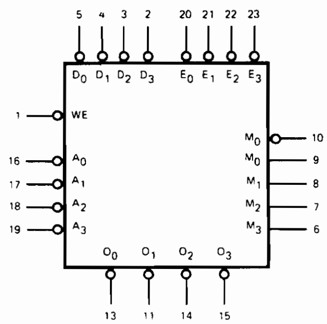
A word is addressed by having an active LOW on the appropriate address line $(\overline{A}_0 - \overline{A}_3)$. Any number of words may be addressed simultaneously.

Data can be written into the memory through the data inputs $(\overline{D}_0 - \overline{D}_3)$ under control of the address inputs and the appropriate bit enable $(\overline{E}_0 - \overline{E}_3)$ when the write enable $(\overline{WE})$ is LOW.

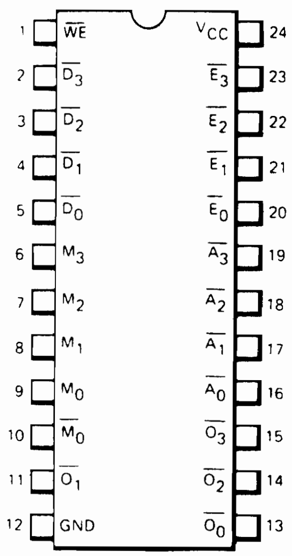
Reading can occur either during an equality search or a write operation. If a single word is addressed that word will appear at the data outputs $(\overline{O}_0 - \overline{O}_3)$. If multiple addressing is used, the word appearing at the data output is the AND (positive logic) or the OR (negative logic) of the addressed words.

All outputs are uncommitted collectors allowing maximum flexibility in output connection. In many applications, such as memory expansion, the outputs of many of these devices can be tied together. In other applications the wired-OR is not used. In either case, an external pull up resistor must be used to attain a HIGH at an output.

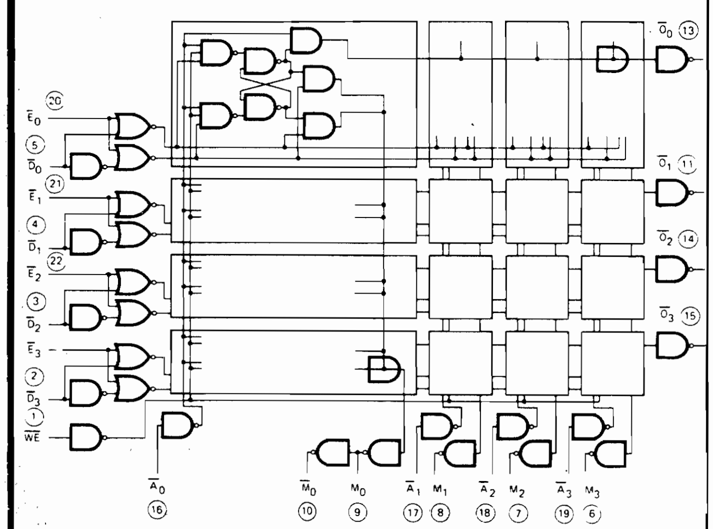
Logic Symbol



Pin Configuration



Logic Diagram

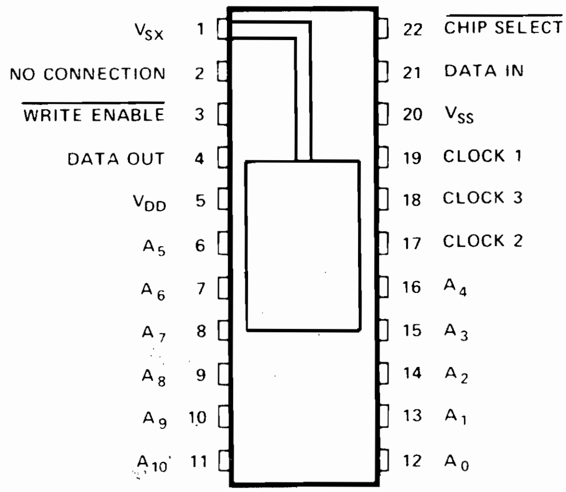


○ = PIN NUMBERS

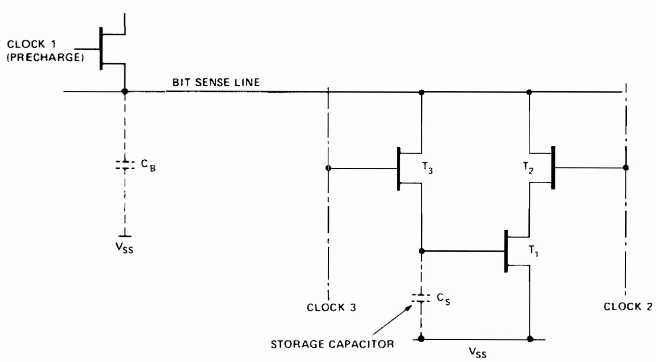
100000214

2048-Bit MOS LSI Random Access Memory

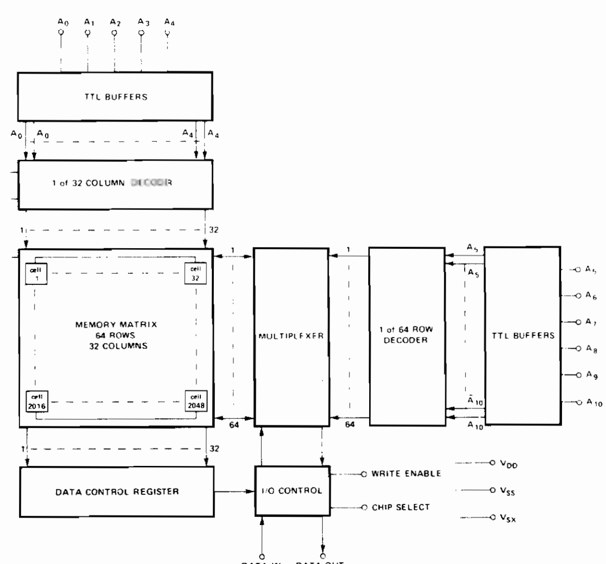
Pin Configuration



Schematic



Block Diagram



The 100000214 is a dynamic MOS random access memory device which utilizes the gate capacitance of a MOS device as a storage medium. The storage cell consists of the storage device T_1, the read select device T_2 and the write select device T_3.

The cycle begins with the negative transition of clock 1. During this time precharge is taking place. In addition, the address inputs, which must be stable during the last 65ns of clock 1 are inverted and amplified. At the end of clock 1 the internal address lines become stable. One of 64 row decoders and one of 32 column decoders are activated during t_{12}, the clock 1 to clock 2 delay time.

Clock 2, the read clock, is channeled by the decoders to the addressed column where T_2, the read select device, is turned on. The condition of the storage device T_1, (on or off) can now be sensed by the bit sense line. The addressed bit sense line is multiplexed to the I/O control circuit which then generates the Data Out. Data In, which must be valid 50ns before clock 3, is conditioned and amplified in the I/O control circuit. During clock 3, the write driver transmits the input data through the multiplexer to the addressed bit sense line.

Clock 3, the write clock, is channeled by the decoders to the addressed column where T_3, the write select device, is turned on. Any information on the bit sense line is, therefore, transferred to the C_S, the gate capacitance of the storage device.

The refresh cycle consists of clock 1, clock 2 and clock 3. Clock 1 precharges the bit sense line. Clock 2 senses the status of the storage device T_1, which is operating in the inverter mode, and places the inverted state of the storage device on the bit sense line. Clock 3, by turning on T_3, transfers the information from the bit sense line to the storage device. Note, each refresh cycle will result in the inversion of the stored data. To refresh all 2048 cells, each of the 32 columns must be selected for a refresh cycle by exercising all 32 combinations of the low order addresses (A_0 - A_4).

The read cycle may consist only of clock 1 and clock 2. Since each refresh cycle inverts the data in the storage cells in an accessed column, a control circuit, the Data Control Register, is used. The Data Control Register, which is basically another set of memory cells, is slaved

Continued ....

100000214

Continued

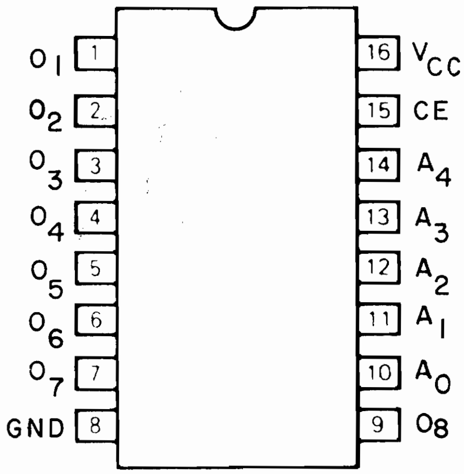
to the memory array. The state of the Data Control Register will provide information as to whether a column of storage cells is in a non-inverting or inverting state.

Clock 1 of the read cycle precharges the device. Clock 2 is transmitted by the column decoders to the addressed column. At this time, data from both the storage cell and the Data Control Register is sensed. The row multiplexer transfers the data from the addressed row to the I/O Control circuit. In the I/O Control circuit, an exclusive-OR function of the data from the memory array and the Data Control Register is performed. The output of the exclusive-OR is then amplified and presented to the Data Out pin. The output data is held in a register until the initiation of the next memory cycle. A new memory cycle may begin 20ns after clock 2 has returned to a positive state. The 100000214 is a non-inverting device; i.e., TTL "high" Data-In will result in an output high current.

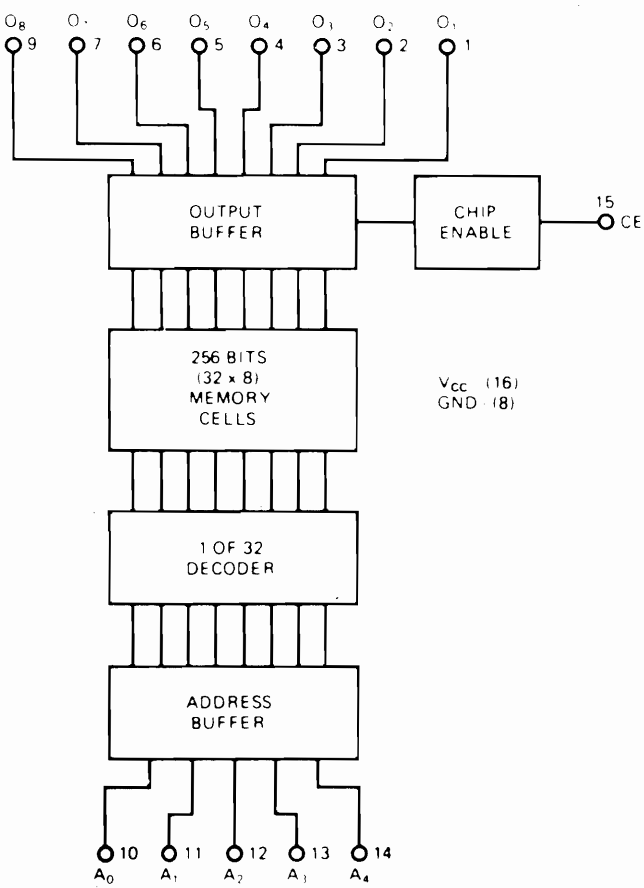
The write cycle consists of clock 1, clock 2 and clock 3. During clock 1 the precharge operation takes place. During clock 2 the Data Control Register is read to determine whether the accessed column is in a true or inverted state. At the beginning of clock 3 the exclusive-OR function of Data-In and the content of the Data Control Register is performed in the I/O Control circuit. The output of the input exclusive-OR is then amplified and transmitted to the addressed cell by the write-driver. A new memory cycle may begin 20ns after clock 3 has returned to the positive state.

100000140 100000141 100000142 100000148 100000149 100000215 100000216 100000217 100000218 100000219 100000269 100000270 100000271 100000272 100000273 100000274 100000275 100000276 100000277 100000278 100000279 100000280 100000499 100000500

Pin Configuration



Functional Block Diagram



256-Bit Bipolar Read Only Memory

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

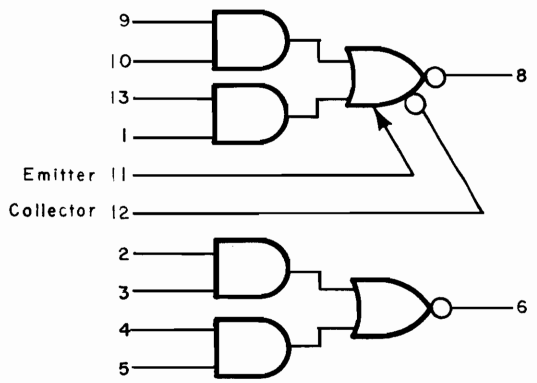
Memory expansion is simple; three-state outputs are provided on the 100000215; uncommitted collector outputs are provided on all other devices. Each device has on-chip address decoding and chip enable. The memory is fabricated with all logic level zeroes(low); logic level ones (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

REV. 03

100000221

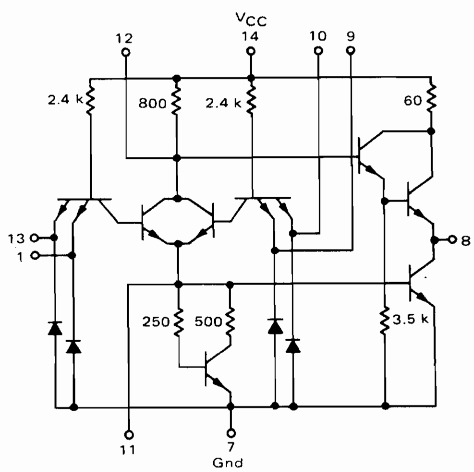
Expandable Dual 2-Wide 2-Input AND-OR-Invert Gate

Logic Diagram



Circuit Schematic

1/2 OF CIRCUIT SHOWN†



†Other half of circuit omits expander inputs.

Logic Diagram

Positive Logic:

$$\overline{8 = (9 \cdot 10) + (13 \cdot 1) + (\text{Expanders})}$$

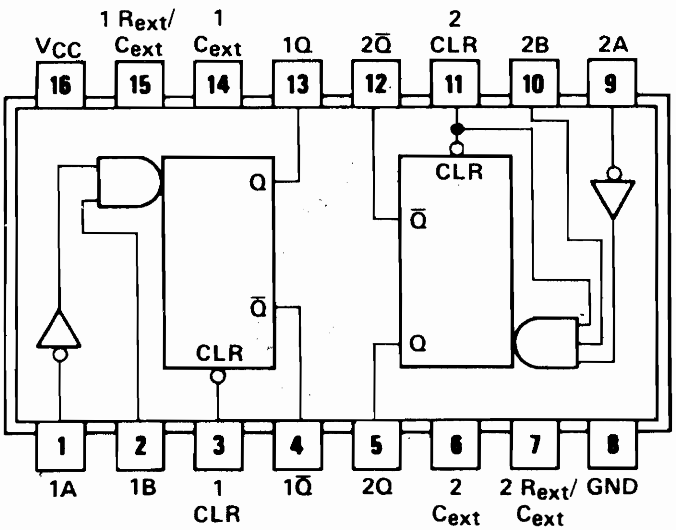
Negative Logic:

$$\overline{8 = (9 + 10) \cdot (13 + 1) \cdot (\text{Expanders})}$$

One side of this dual device consists of two 2-input AND gates ORed together and driving an output inverter. The other side consists of two 2-input gates ORed together, driving an output inverter, and the ORing nodes are available for expansion.

100000222

Pin Configuration



Dual Retriggerable Monostable Multivibrator with Clear

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Truth Table

Inputs			Outputs	
Clear	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

Notes:

H = high level (steady state).
L = low level (steady state).
↑ = transition from low to high level.
↓ = transition from high to low level.
⊓ = one high-level pulse.
⊔ = one low-level pulse.
X = irrelevant (any input, including transitions).

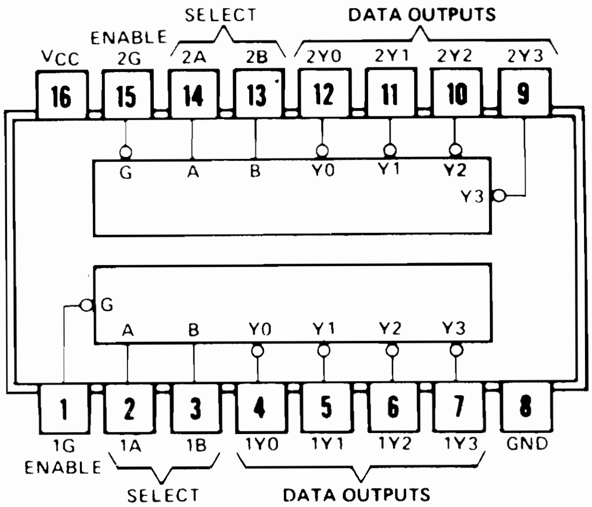
An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

REV. 03

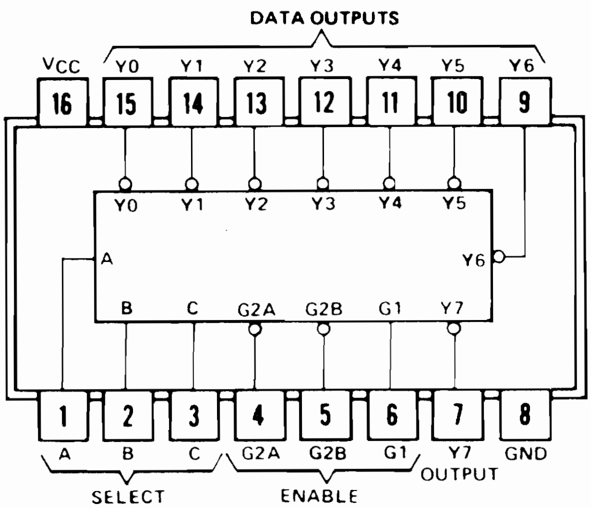
100000185 100000223

Pin Configurations

100000185



100000223



Decoders-Demultiplexers

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Function Table - 100000223

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level; L = low level; X = irrelevant

Function Table - 100000185
(Each Decoder/Demultiplexer)

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level; L = low level; X = irrelevant

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

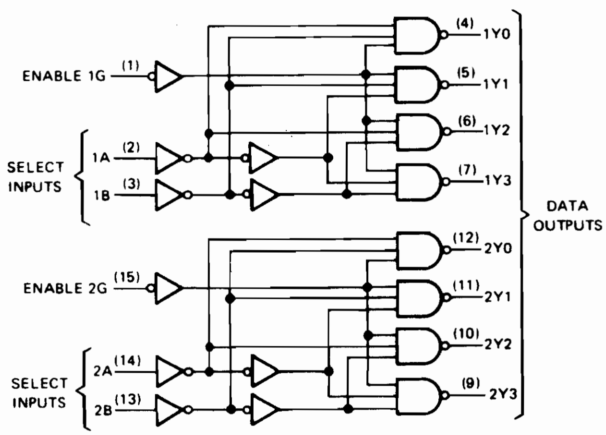
Continued....

100000185 100000223

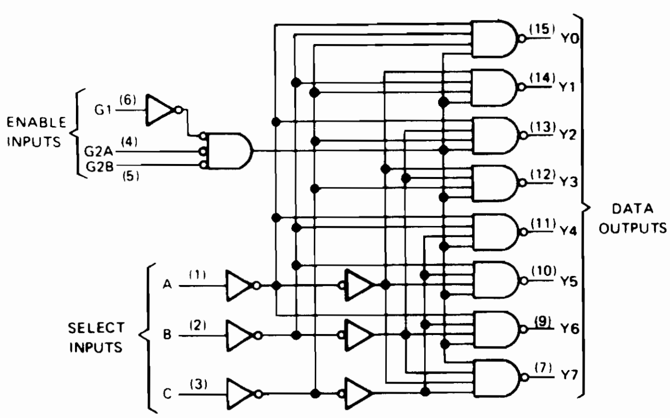
Continued

Logic Diagrams

100000185



100000223



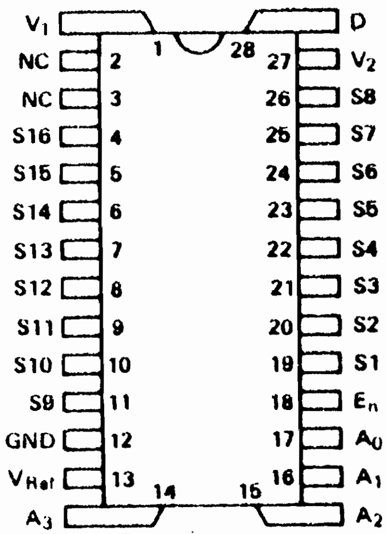
The 100000223 decodes one-of-eight lines, depending on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 100000185 is comprised of two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

100000224

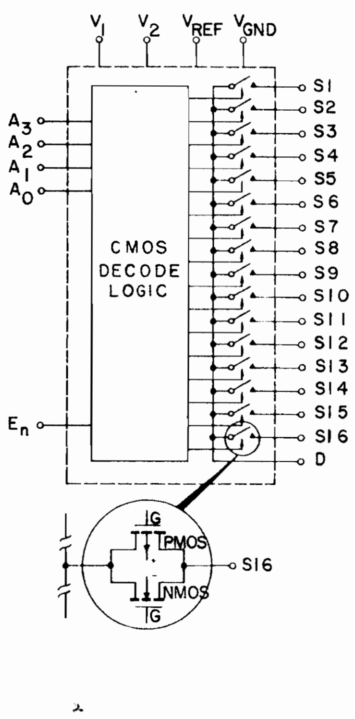
16-Channel Analog Multiplexer Complementary MOS (CMOS)

Pin Configuration



TOP VIEW
V1 COMMON TO SUBSTRATE

Functional Diagram



Decode Truth Table

A_3	A_2	A1	A0	En	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} > 2.4V$

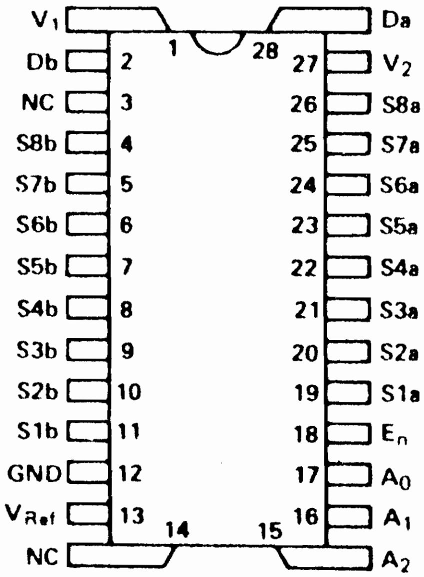
Logic "0" = $V_{AL} < 0.8V$

The 100000224 is a single-pole 16-position (plus OFF) electronic switch array which employs 16 pairs of complementary MOS (CMOS) field-effect transistors designed to function as analog switches. In the ON condition each switch will conduct current in either direction; in the OFF condition each switch will block voltages up to 30V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 4-bit binary word input plus an Enable-Inhibit input. The truth table shows the binary word required to select any one of the 16 switch positions, provided a positive logic "1" is present at the Enable input. With logic "0" at the Enable input all switches will be OFF. The logic decoder and the Enable inputs will recognize voltages between -0.3 and 0.8V as logic "0" voltages, and voltages between 2 and 15V as logic "1" voltages. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain special P-MOS circuits. Switch action is break-before-make.

100000225

8-Channel Differential Analog Multiplexer Complementary MOS (CMOS)

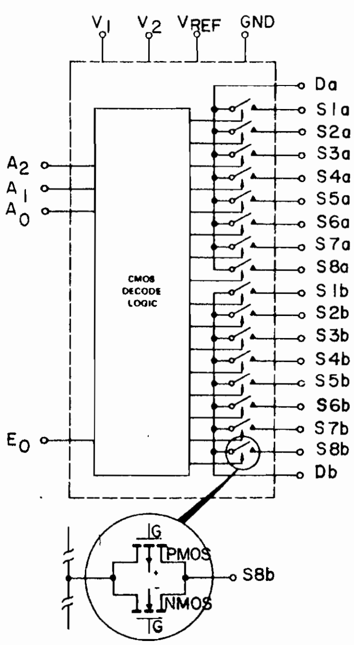
Pin Configuration



TOP VIEW

V_1 COMMON TO SUBSTRATE

Functional Diagram



Decode Truth Table

A_2	A_1	A_0	E_n	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "1" = $V_{AH} > 2.4V$

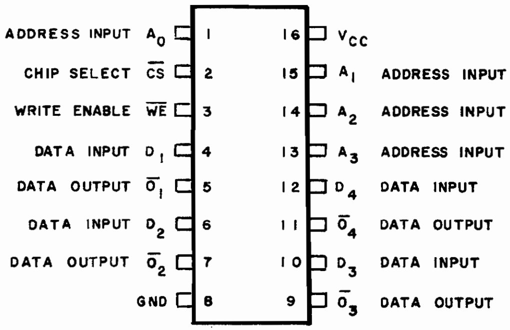
Logic "0" = $V_{AL} < 0.8V$

The 100000225 is a double-pole 8-position (plus OFF) electronic switch array which employs 16 pairs of complementary MOS (CMOS) field-effect transistors designed to function as analog switches. In the ON condition each switch will conduct current in either direction; in the OFF condition each switch will block voltages up to 30V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word input plus an Enable-Inhibit input. The truth table shows the binary word required to select any one of the eight switch positions, provided a positive logic "1" is present at the Enable input. With logic "0" at the Enable input all switches will be OFF. The logic decoder and the Enable inputs will recognize voltages between -0.3 and 0.8V as logic "0" voltages, and voltages between 2 and 15V as logic "1" voltages. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain special P-MOS circuits. Switch action is break-before-make.

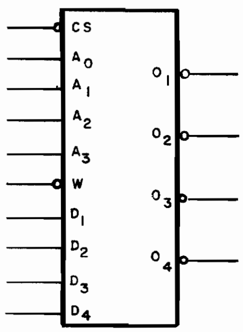
100000226

High Speed Fully Decoded 64-Bit Memory

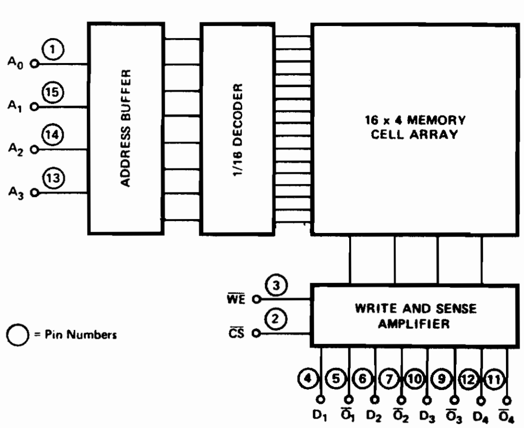
Pin Configuration



Logic Symbol



Block Diagram



Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Pin Names

D_1-D_4	Data Inputs
A_0-A_3	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select Input
$\overline{O_1}$-$\overline{O_4}$	Data Outputs
V_{CC}	Power (+5V)

The 100000226 is a high speed, fully decoded 64-bit random access memory, using Schottky barrier diode clamped transistors. Organization is 16 words by 4 bits.

An unselected chip will not generate noise at its output during writing of a selected chip. The output is held high on an unselected chip regardless of the state of the read/write signal.

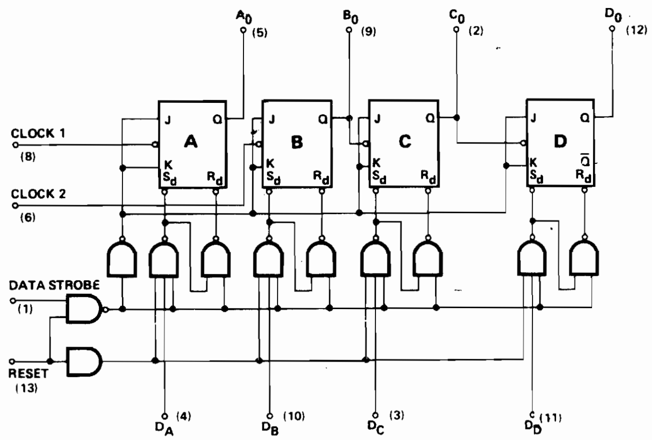
The storage cells are addressed through an on-chip 1 of 16 binary decoder using four input address leads.

A separate Chip Select lead allows selection of an individual package when outputs are OR-tied. In addition to the address leads and the Chip Select lead, there is a write input which allows data presented at the data leads to be entered at the addressed storage cells.

100000080 100000227

Presettable High Speed Binary Counter

Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

Input	A_0	B_0	C_0	D_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

The 100000080 Presettable High Speed Binary Counter may be connected as a divide-by-two, four, eight or sixteen counter.

This device has strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. This unit is provided with a reset input which is common to all four bits. A "0" on the reset lines produces "0" at all four outputs.

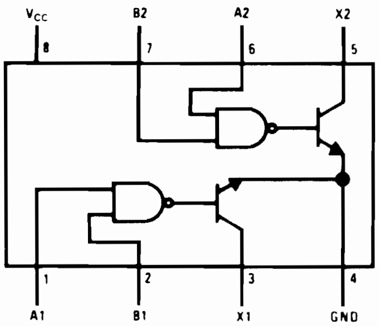
The counting operation is performed on the falling (negative-going) edge of the input clock pulse.

Note: The 100000227 is a Schottky device.

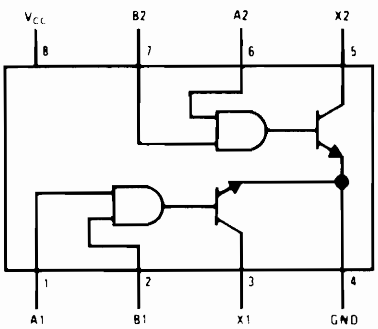
100000228 100000247 100000238 100000154 100000117

Dual Peripheral Drivers

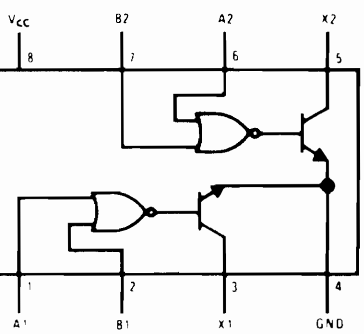
Pin Configurations



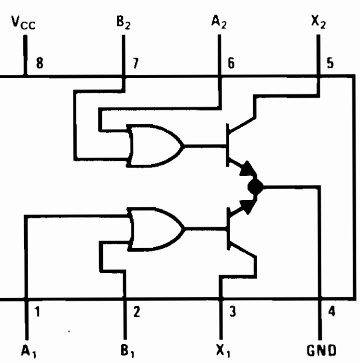
100000247/100000238



100000154



100000117



100000228

V_{CC} = Pin 8
Gnd = Pin 4

Truth Tables

100000247 and 100000238

Positive logic: AB=X

A	B	Output X*
0	0	0
1	0	0
0	1	0
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000154

Positive logic: $\overline{AB}$=X

A	B	Output X*
0	0	1
1	0	1
0	1	1
1	1	0

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000117

Positive logic: A + B = X

A	B	Output X*
0	0	0
1	0	1
0	1	1
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

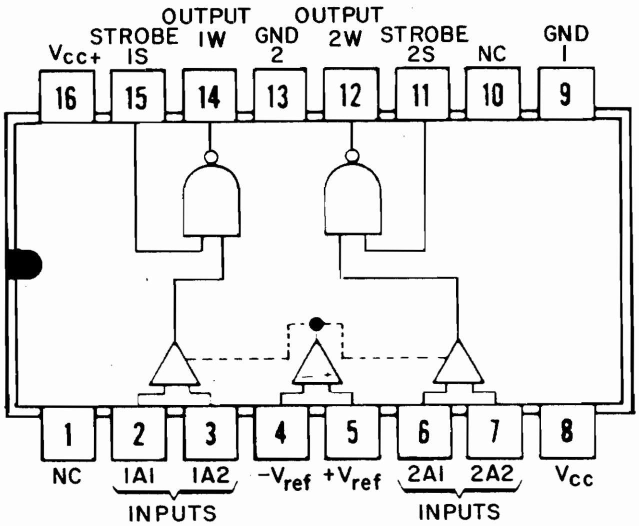
100000228
Truth Table

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible.

100000118 100000229 100000298 100000299

Pin Configuration



Dual Sense Amplifiers

Logic Diagram/Pin Designations

V_{CC+} = Pin 16
V_{CC} = Pin 8
Gnd 1 = Pin 9
Gnd 2 = Pin 13
NC = No internal connection

Positive logic: $W = \overline{AS}$

Truth Table

Inputs A	Inputs S	Output W
H	H	L
L	X	H
X	L	H

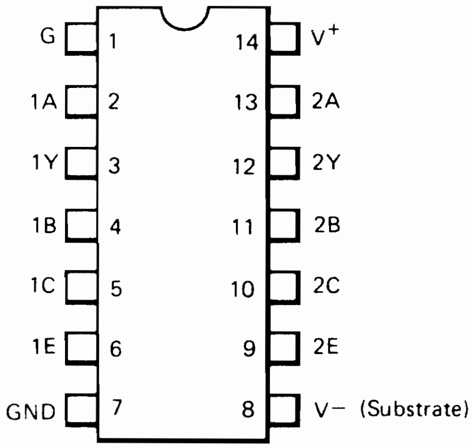
Definition of logic levels:

Input	H	L	X
A*	$V_{ID} \geq V_{Tmax}$	$V_{ID} \leq V_{Tmin}$	Irrelevant
S	$V_I \geq V_{IHmin}$	$V_I < V_{ILmax}$	Irrelevant

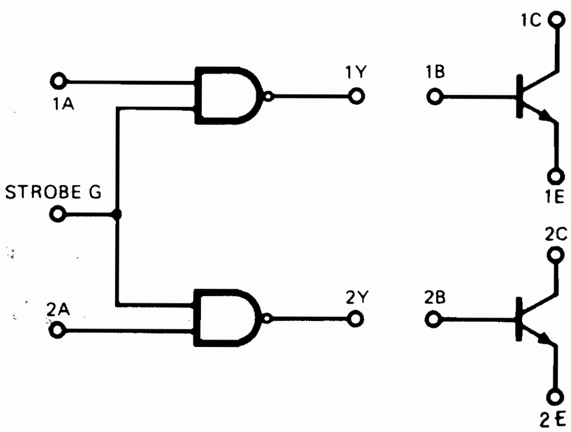
* A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

100000231 100000385

Pin Configuration



Functional Block Diagram



Dual Peripheral Driver

Pin Designations

V+ = Pin 14

V- = Pin 8

Gnd = Pin 7

REV. 03

100000232

1024-Bit Field Programmable Bipolar PROM

Pin Designations

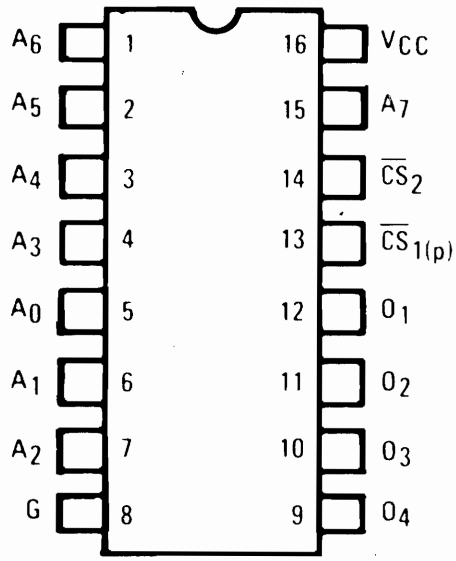
V_{CC} = Pin 16

Gnd = Pin 8

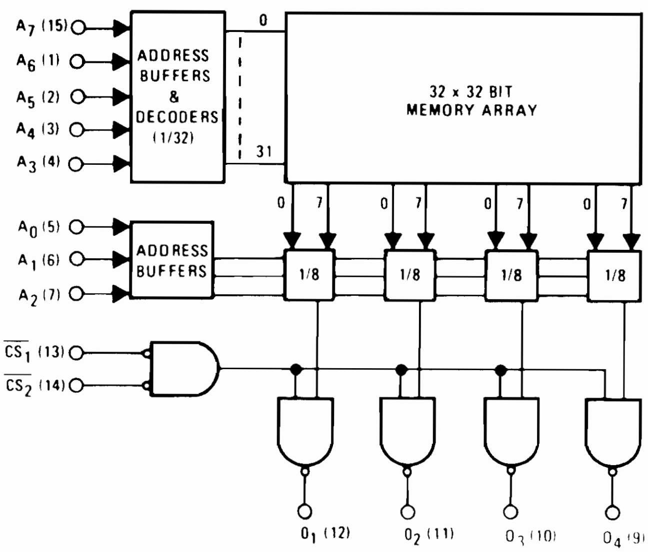
The 100000232 is a fully decoded, high speed, 1024-bit, field programmable ROM, organized as 256 words by 4 bits per word. The device has an open collector output.

This PROM is supplied with all bits storing a logical "1" (output high) and can be selectively programmed for a logical "0" (output low). The addressing scheme for programming and reading the information in the system is the same.

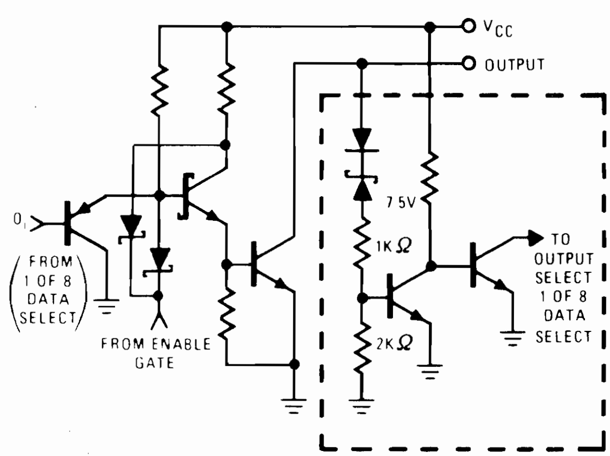
Pin Configuration



Functional Block Diagram



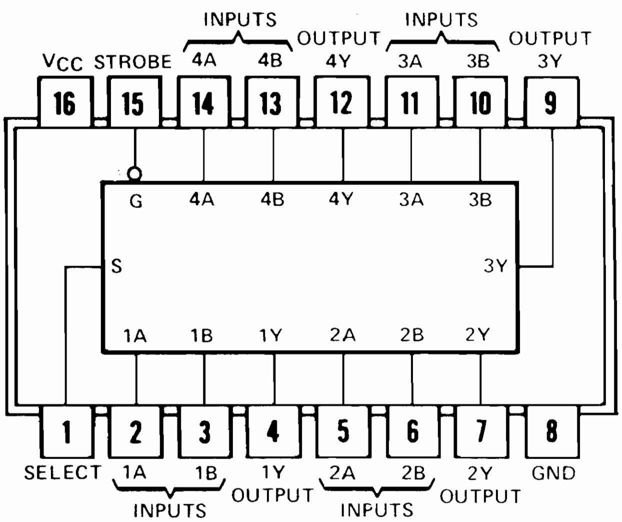
Schematic Output Circuit



100000233 100000240

Quadruple 2-Line-To-1-Line Data Selector/Multiplexer

Pin Configuration



Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Positive logic:

Low logic level at S selects A inputs.
High logic level at S selects B inputs.

Function Table

Inputs				Output
Strobe	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

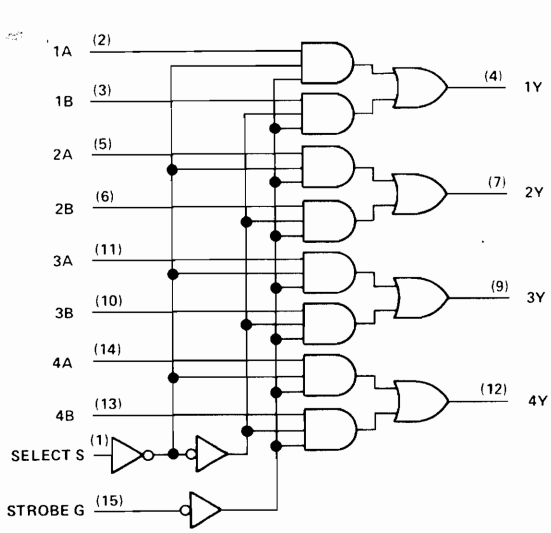
Notes:

H = high level; L = low level; X = irrelevant.

These monolithic data selectors/multiplexors contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. These devices present true data.

Note: The 100000233 is a Schottky device.

Logic Diagram

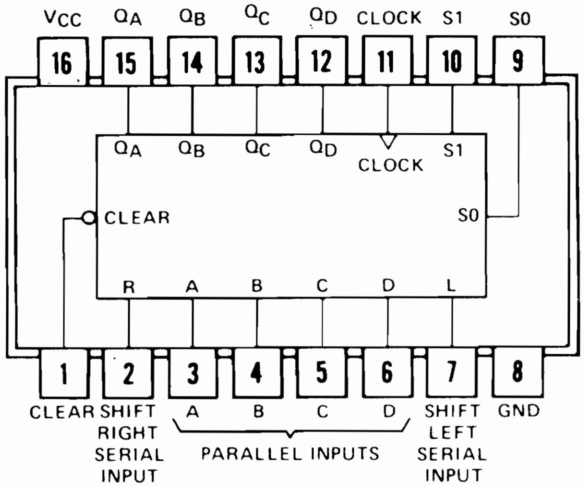


REV. 03

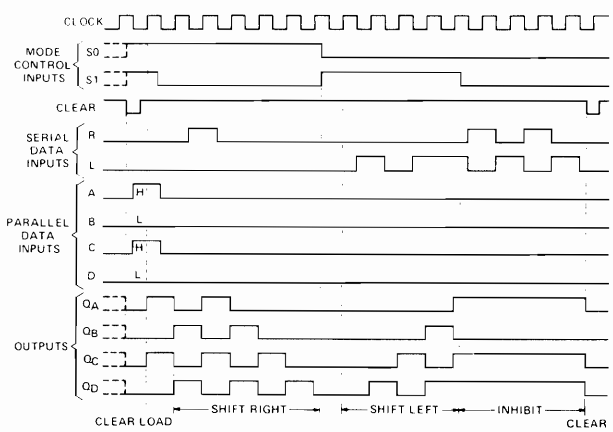
100000135 100000234

4-Bit Bidirectional Universal Shift Registers

Pin Configuration



Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences



Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Function Table

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S_1	S_0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state).

L = low level (steady state).

X = irrelevant (any input, including transitions).

↑ = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the most recent ↑ transition of the clock.

Note: The 100000234 is a Schottky device.

The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation:

Parallel (Broadside) Load

Shift Right (in the direction Q_A toward Q_D)

Shift Left (in the direction Q_D toward Q_A)

Inhibit Clock (Do nothing)

Continued....

100000135 100000234

Continued

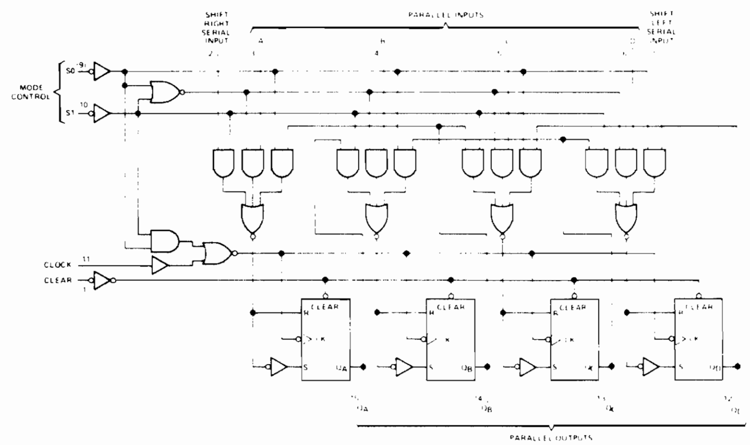
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

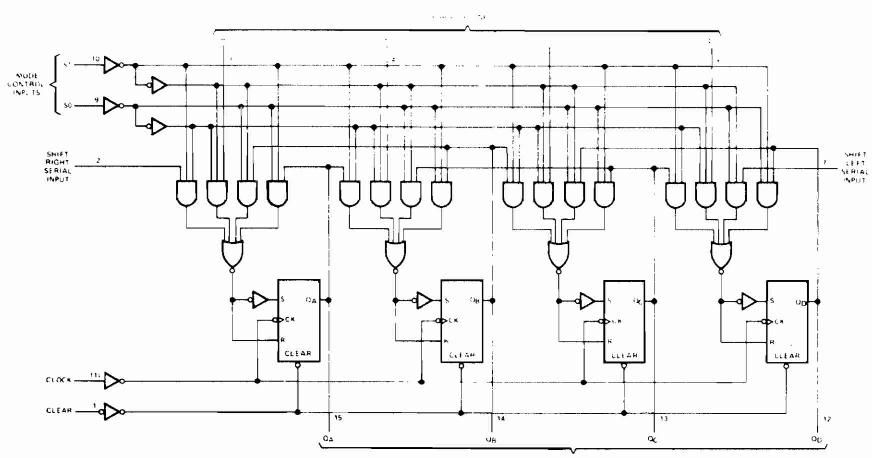
Clocking of the flip-flop is inhibited when both mode control units are low. The mode controls of the 100000135 should be changed only while the clock input is high.

Logic Diagrams

100000135



100000234

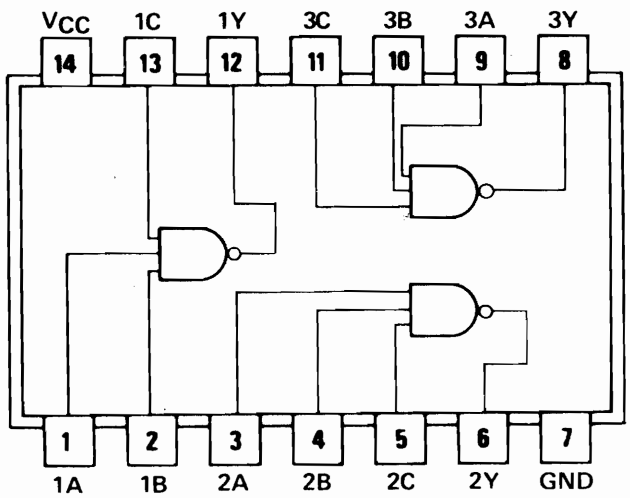


.... dynamic input activated by a transition from a high level to a low level.

100000235 100000327 100000339

Triple 3-Input Positive-NAND Gate

Pin Configuration



Logic Diagram/Pin Designations

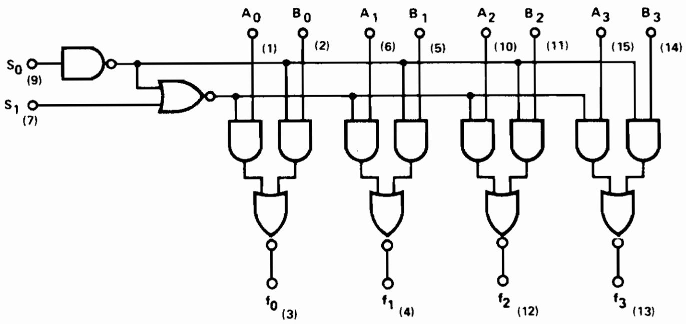
V_{CC} = Pin 14
Gnd = Pin 7

Positive logic: $Y = \overline{ABC}$

Note: The 100000235 is a Schottky device.

100000236

Logic Diagram



2-Input, 4-Bit Digital Multiplexer

Logic Diagram/Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Truth Table

S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

This 2-Input, 4-Bit Digital Multiplexer features inverting data paths.

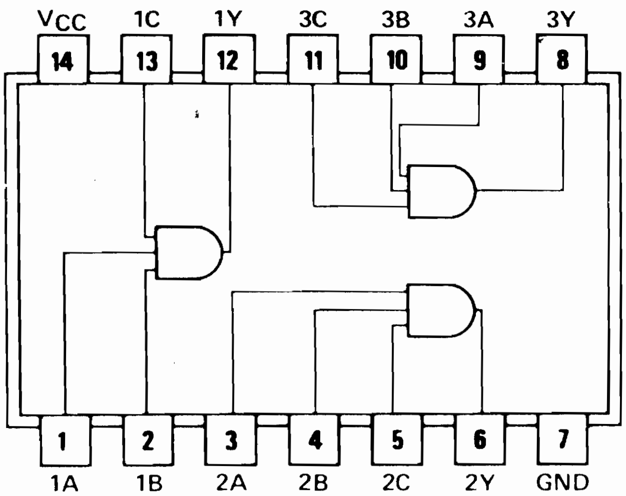
The 100000236 has open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as forty four-bit words can be multiplexed by using twenty of these devices in the WIRED-AND mode.

The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

Note: The 100000236 is a Schottky device.

100000237

Pin Configuration



Triple 3-Input Positive-AND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Positive logic: Y = ABC

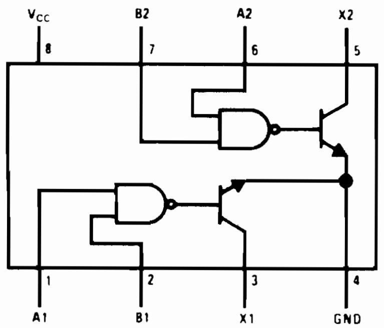
Note: The 100000237 is a Schottky device.

REV. 03

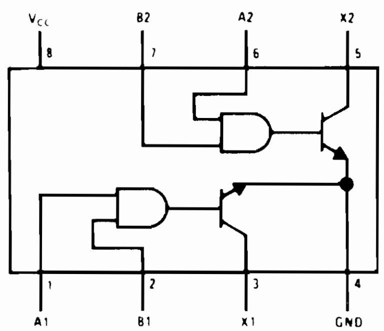
100000228 100000247 100000238 100000154 100000117

Dual Peripheral Drivers

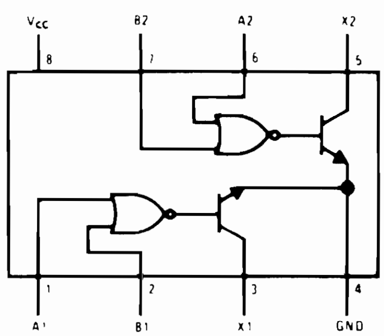
Pin Configurations



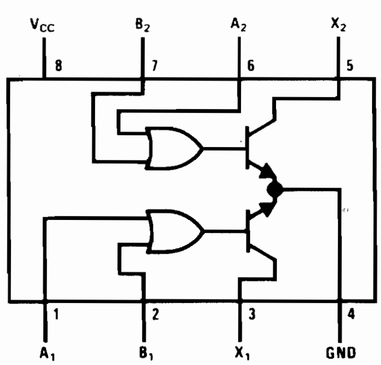
100000247/100000238



100000154



100000117



100000228

V_{CC} = Pin 8
Gnd = Pin 4

Truth Tables

100000247 and 100000238

Positive logic: AB=X

A	B	Output X*
0	0	0
1	0	0
0	1	0
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000154

Positive logic: $\overline{AB}$=X

A	B	Output X*
0	0	1
1	0	1
0	1	1
1	1	0

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000117

Positive logic: A + B = X

A	B	Output X*
0	0	0
1	0	1
0	1	1
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000228
Truth Table

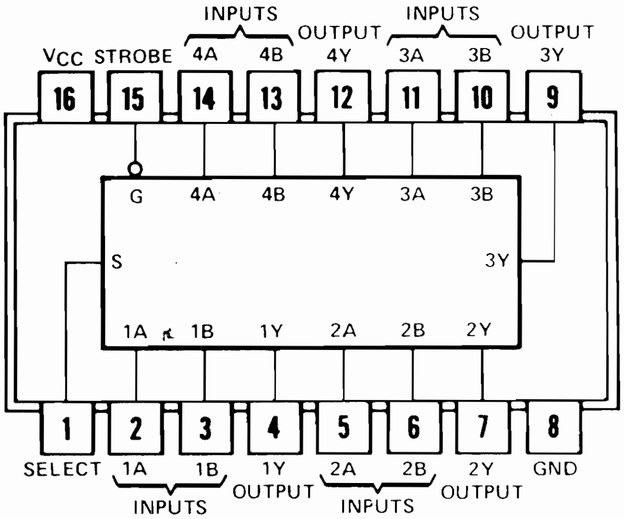
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible.

100000233 100000240

Quadruple 2-Line-To-1-Line Data Selector/Multiplexer

Pin Configuration



Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Positive logic:

Low logic level at S selects A inputs.
High logic level at S selects B inputs.

Function Table

Inputs				Output
Strobe	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

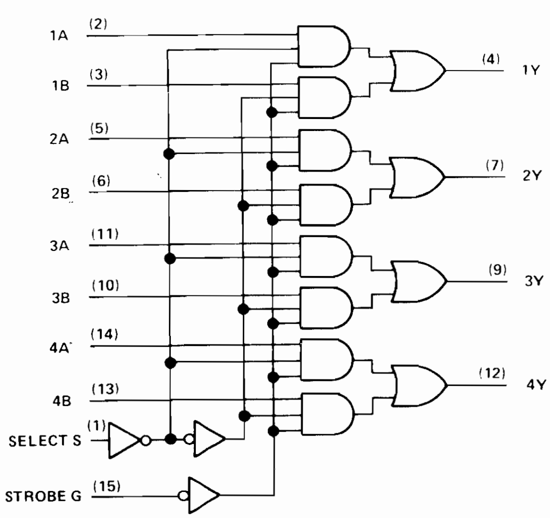
Notes:

H = high level; L = low level; X = irrelevant.

These monolithic data selectors/multiplexors contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. These devices present true data.

Note: The 100000233 is a Schottky device.

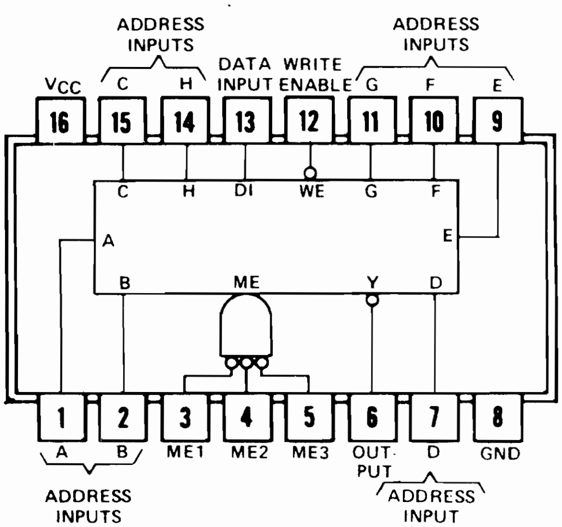
Logic Diagram



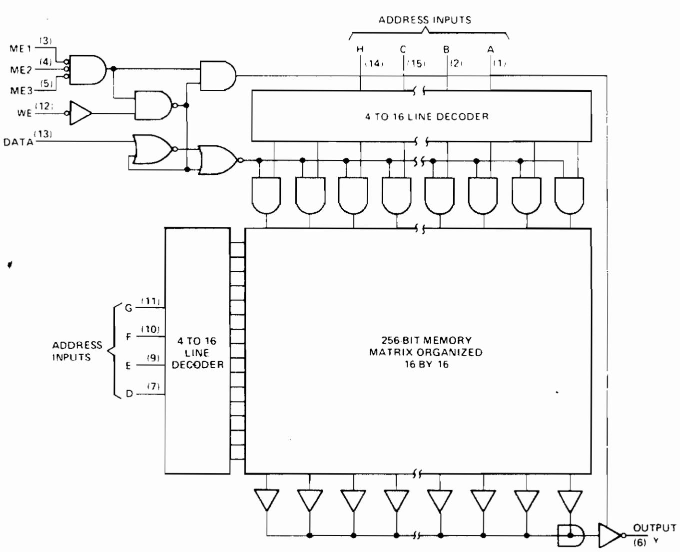
REV. 03

100000241

Pin Configuration



Functional Block Diagram



256-Bit Read-Write Memory With 3-State Outputs

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Positive logic:

Data out is complement of data which was applied at data input.

Function Table

Function	Inputs: Memory Enable*	Inputs: Write Enable	Output
Write (Store complement of data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = high level
L = low level
X = irrelevant
* For memory enable:

L = all ME inputs low
H = one or more ME inputs high

This 256-bit active-element memory is a monolithic TTL array organized as 256 words of one bit each. It is fully decoded and has three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

Write Cycle

The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write enable input is low, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle

The stored information (complement of information applied at the data input during the write

Continued ....

100000241

Continued

cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be in the high-impedance state.

The high capacitive drive capability of the three-state bus-connectable output permits expansion up to 66, 304 words of N-bits without additional output buffering. The functional capability of the output being at a high impedance during writing and the data input being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Word Capacity Vs. Loads

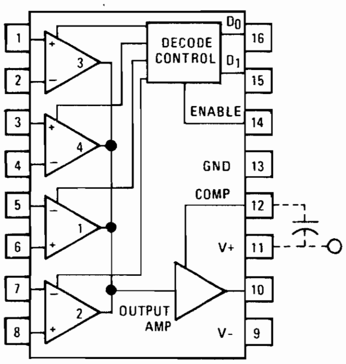
Loads	Maximum Number of Common Outputs	Maximum Number of Words
1	259	66, 304
2	220	56, 320
3	180	46, 080
4	140	35, 840
5	100	25, 600
6	60	15, 360
7	20	5, 120

Note: The 100000241 is a Schottky device.

100000242

Four Channel Programmable Amplifier

Pin Configuration



Truth Table

D_1	D_0	EN	Selected Channel
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	None

This operational amplifier has four identical input stages, any one (or none) of which may be electronically connected to the single output stage. The "ON" channel is selected through DTL/TTL compatible address inputs. The unselected amplifier inputs are effectively "floating".

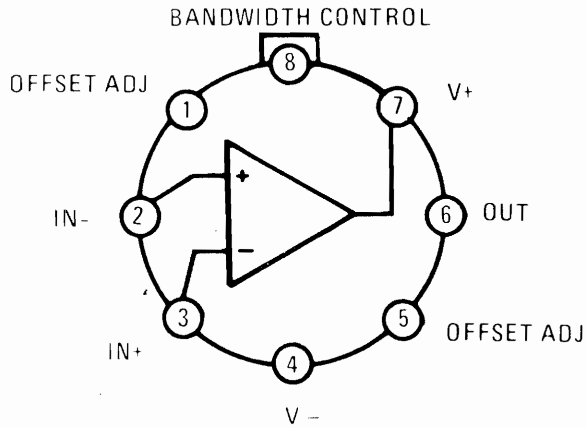
This device can be used as an analog signal selector, sampler or multiplexer with built in buffering or signal conditioning. By connecting different feedback networks from the output to each input pair, it can be used as a single or multiple channel amplifier with programmable feedback characteristics.

100000243

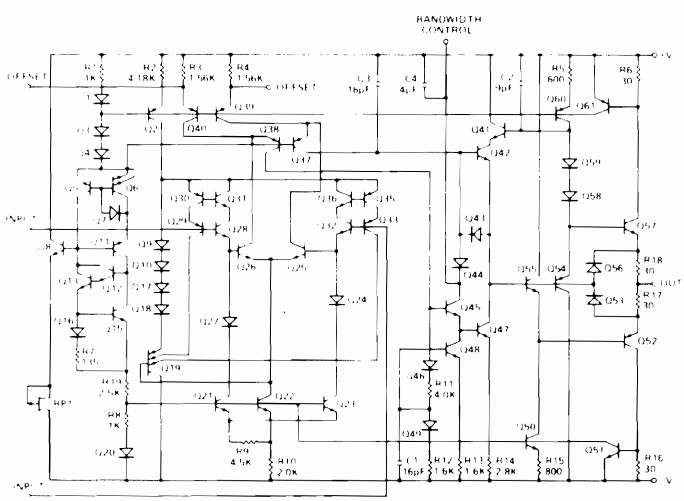
Wide Band, High Impedance Operational Amplifier

This operational amplifier has very low input bias current and is intended for use as a high impedance comparator and a wide band amplifier. The device provides very high gain, very high slew rate and output short circuit protection.

Pin Configuration



Schematic



100000244

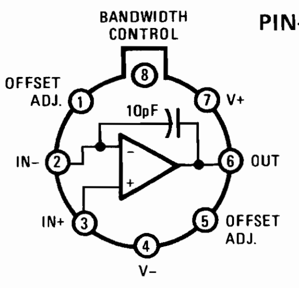
High Slew Rate F.E.T. Input Operational Amplifier

This operational amplifier combines very high slew rate and wide bandwidth with ultra-low input current and high input resistance.

The device may be operated inverting or non-inverting. External compensation is required only when operated at closed loop gains less than three. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

Pin Configuration

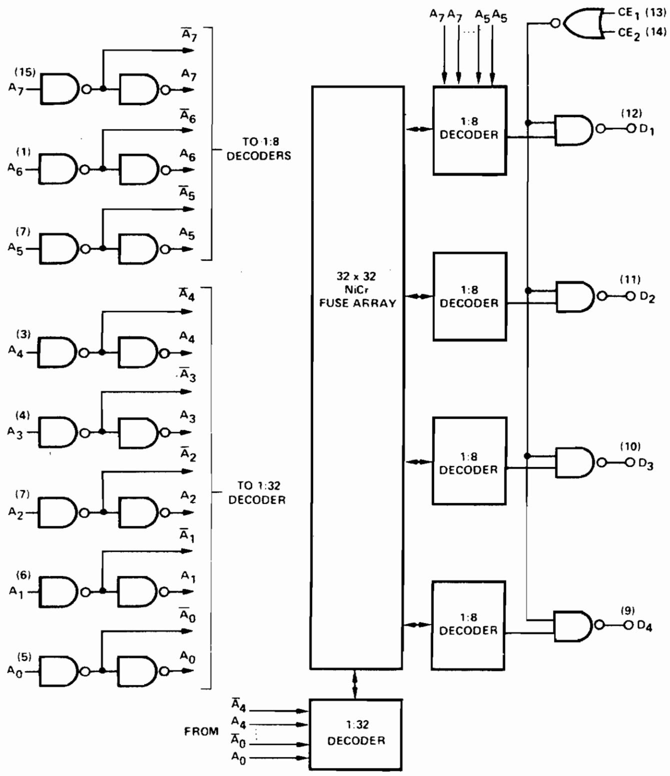
PIN-OUT



(TOP VIEW)

100000245

Functional Block Diagram



1024-Bit Bipolar Programmable ROM (256 × 4 PROM, Open Collector)

Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

The 100000245 is a Bipolar 1024 Bit Read Only Memory organized as 256 words by 4 bits per word, with open collector outputs. This device is field-programmable.

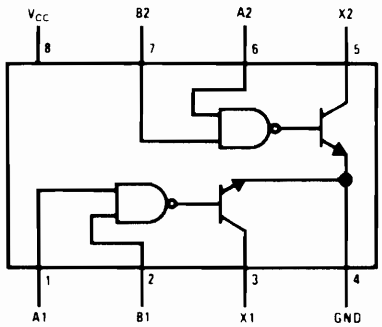
Two chip enable lines are provided and the outputs are bussable to allow for memory expansion capability.

Note: The 100000245 is a Schottky device.

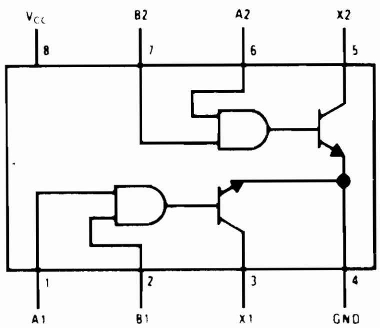
100000228 100000247 100000238 100000154 100000117

Dual Peripheral Drivers

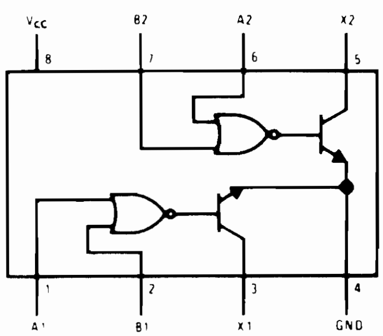
Pin Configurations



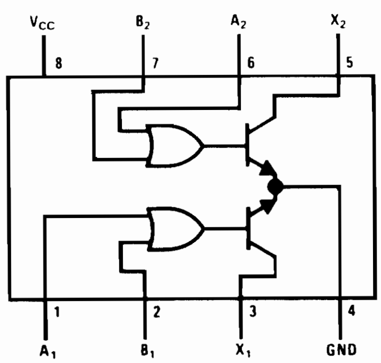
100000247/100000238



100000154



100000117



100000228

V_{CC} = Pin 8
Gnd = Pin 4

Truth Tables

100000247 and 100000238

Positive logic: AB=X

A	B	Output X*
0	0	0
1	0	0
0	1	0
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000154

Positive logic: $\overline{AB}$=X

A	B	Output X*
0	0	1
1	0	1
0	1	1
1	1	0

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000117

Positive logic: A + B = X

A	B	Output X*
0	0	0
1	0	1
0	1	1
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

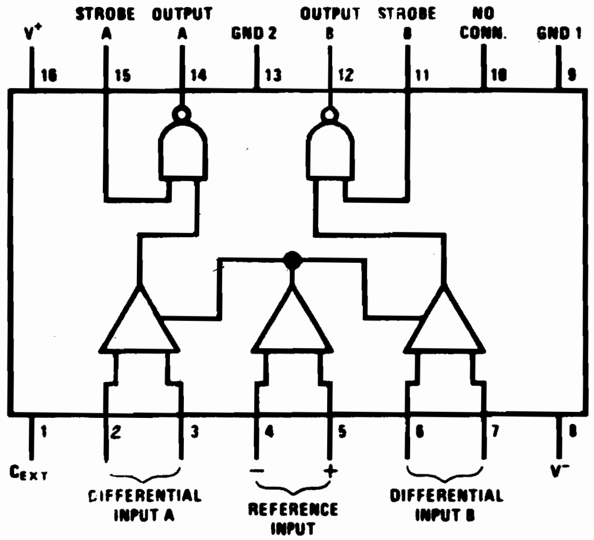
100000228
Truth Table

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible.

100000248

Pin Configuration



Sense Amplifier

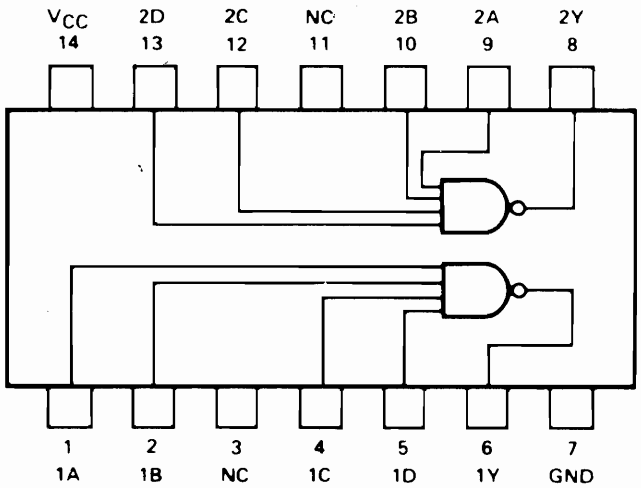
Pin Designations

V+	= Pin 16
V-	= Pin 8
Gnd 1	= Pin 9
Gnd 2	= Pin 13

These dual core sense amplifiers convert bipolar millivolt-level memory sense signals to saturated logic levels. The design employs a common reference input which allows the input threshold voltage level of both amplifiers to be adjusted. Separate strobe inputs provide time discrimination for each channel. Logic inputs and outputs are DTL/TTL compatible.

100000249 100000374

Pin Configuration



Positive-NAND Gate

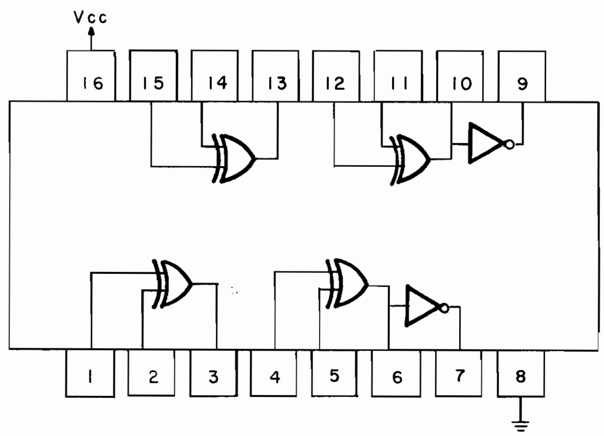
Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Note: The 100000249 is a Schottky device.

100000250

Pin Configuration



Quad Exclusive-OR Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Truth Table

A	B	Z	$\overline{Z}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

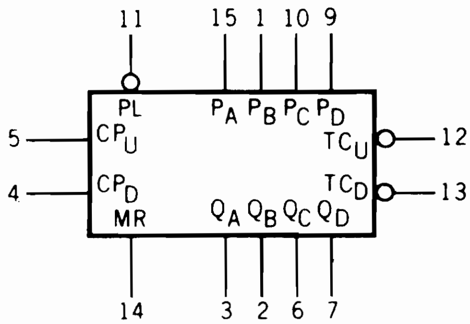
H = High Voltage Level
L = Low Voltage Level

The exclusive OR gate produces an output when the inputs are complementary. Two gates have an additional inverted output which provides directly a compare capability. The Boolean expressions for the gates are: $Z = A\overline{B} + \overline{A}B$; $\overline{Z} = AB + \overline{AB}$.

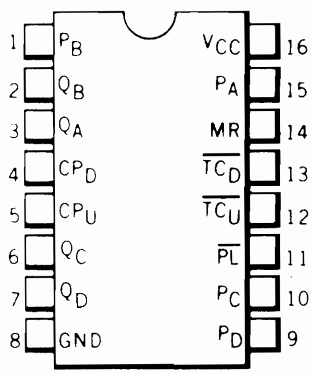
100000252 100000128 100000384

Up/Down Decade and Binary Counters

Logic Symbol

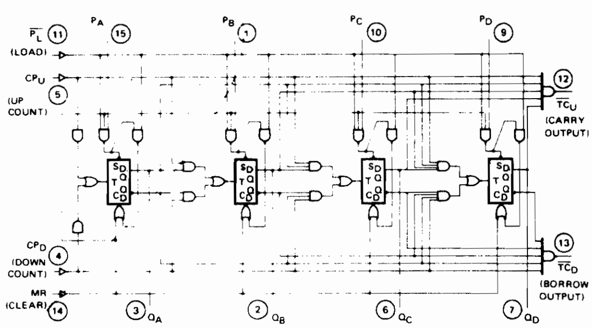


Pin Configuration

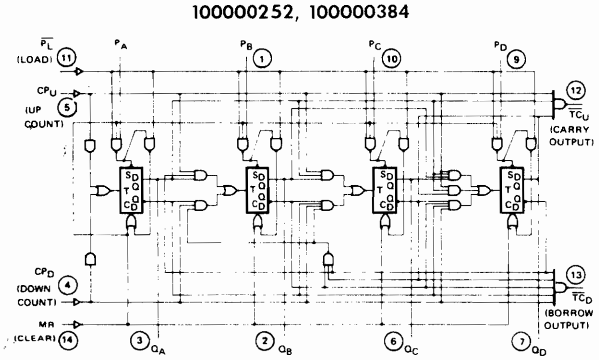


Logic Diagrams

100000128



100000252, 100000384



○ = PIN NUMBER

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Mode Selection
(Both Counters)

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

Notes:

H = High voltage level
L = Low voltage level
X = Don't care condition
CP = Clock pulse.

The 100000252 & 100000384 are synchronous Up/Down BCD Decade Counters and the 100000128 is a synchronous Up/Down 4-Bit Binary Counter. All these counters have separate up/down clocks, parallel load facility, terminal count outputs for multidecade operation and an asynchronous overriding master reset.

These counters can be reset, preset and count up or down. The operating modes are tabulated in the Mode Selection table. The operating modes of both devices are identical; the only difference between the devices is the count sequences.

Counting is synchronous, with the outputs changing state after the Low to High transition of either the Count-Up Clock (CP_U) or Count-Down Clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is High. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are Low simultaneously.) All counters will respond to a clock pulse on either input by changing to the next appropriate state of the count sequence. The state diagram for the 100000252 & 100000384 show the regular sequence and in addition shows the sequence of states if a code greater than nine is present in the counter.

Continued. . . .

100000252 100000128 100000384

Continued

Logic Equations for Terminal Count

100000252 , 100000384

$$TC_U = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot \overline{CP_U}$$

$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

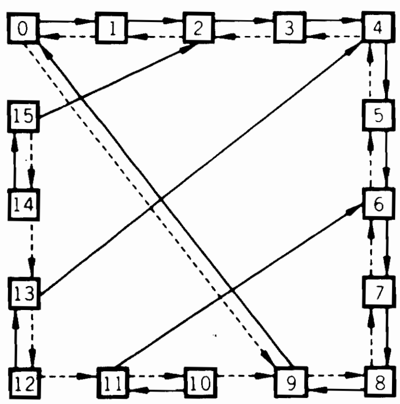
100000128

$$TC_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP_U}$$

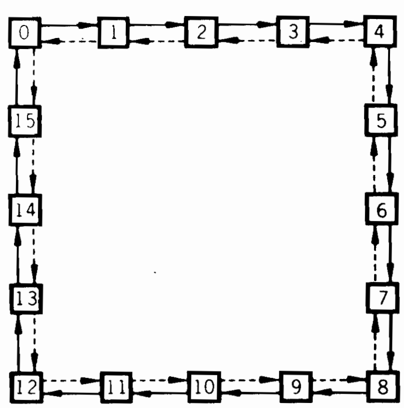
$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

State Diagrams

100000252, 100000384



100000128



COUNT UP ——————
COUNT DOWN -------

All counters have a parallel load (asynchronous) facility which permits the device to be preset. Whenever the parallel load ($\overline{PL}$) input is Low, and Master Reset is Low, the information present on the Parallel Data inputs (P_A, P_B, P_C, P_D) will be loaded into the counters and appear on the outputs independent of the conditions of the clock inputs. When the Parallel Load Input goes High, this information is stored in the counters and when the counters are clocked they change to the next appropriate state in the count sequence. The Parallel Data inputs are inhibited when the Parallel Load is High and have no effect on the counters.

The Terminal Count-Up ($\overline{TC_U}$) and Terminal Count-Down ($\overline{TC_D}$) outputs (carry and borrow, respectively) allow multidecade counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and terminal count-down clock input of the following counter.

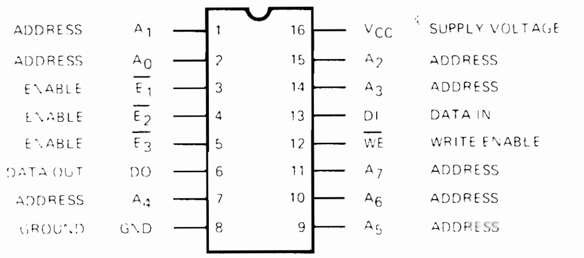
The terminal count-up outputs are Low when their count-up clock inputs are Low and the counters are in state nine (100000252 & 100000384) and state fifteen (100000128). Similarly, the terminal count-down outputs are Low when their count-down clock inputs are Low and both counters are in state zero. Thus, when the 100000252 & 100000384 counters are in state nine and the 100000128 counter is in state fifteen and all are counting up, or all counters are in state zero and counting down, a clock pulse will change the counter's state on the rising edge and simultaneously clock the following counter through the appropriate active Low terminal count output. There are two gate delays per state when these counters are cascaded.

The asynchronous Master Reset input (MR), when High, overrides all input and clears the counters. Master reset overrides parallel load so that when both are activated the counters will be reset. (Obviously, both parallel load and master reset must not be deactivated simultaneously for predictable operation.)

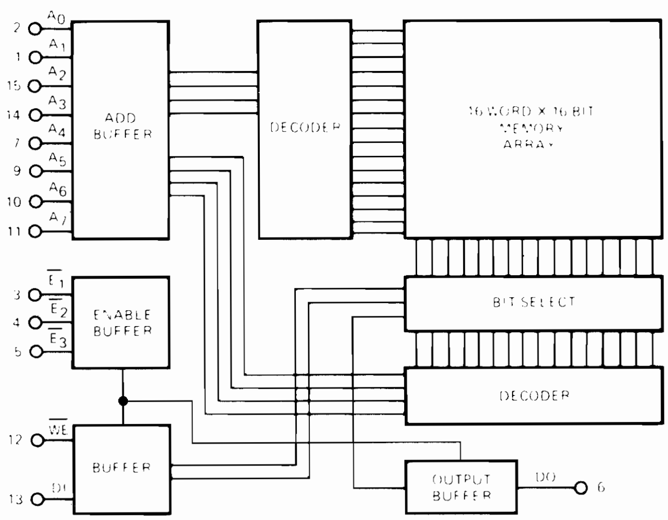
100000255

256 Bit Bipolar Random Access Memory

Pin Configuration



Logic Diagram



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Truth Table

Chip Select	Write Enable	Operation	Output
All Low	Low	Write	Complement of data input
All Low	High	Read	Complement of written data
One or More High	Don't Care	Hold	High

The 100000255 is a fully decoded static bipolar random access memory organized 256 words by 1 bit, with open-collector outputs. The open-collector parts have 3 chip enables for easy expansion to larger size memories.

Memory Operation

Read

The memory is addressed with the A_0-A_7 inputs which select one of the 256 words. The chip is enabled by making all chip enables low. If any or all chip enables are high the chip is disabled. If the write enable is high and the chip is enabled the stored data is read out on the data out pin. The data read out is the complement of the data written in during the write cycle.

Write

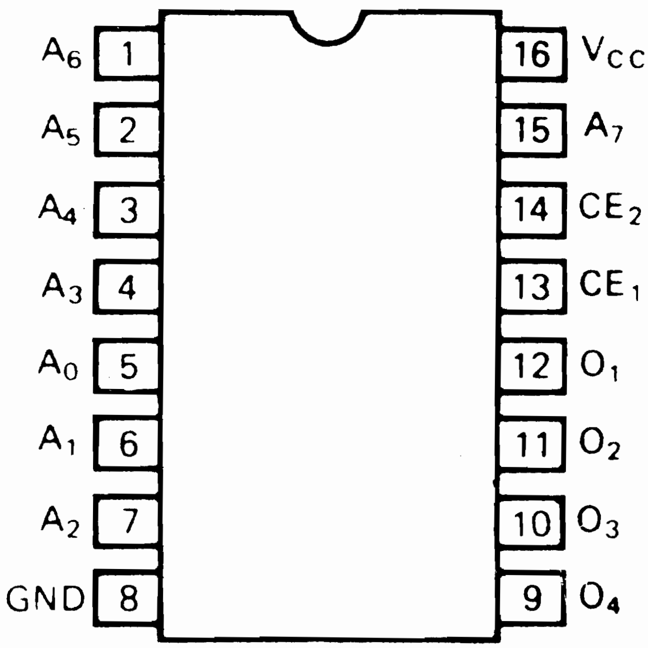
The memory is addressed with the A_0-A_7 inputs which select one of the 256 words. The chip is enabled as in the read cycle. If the write enable is low the data on the data input pin is written into the addressed word. The data out of the memory during the write cycle is the complement of the data written in. This allows checking of the stored data during the write cycle.

Memory Expansion Rules

1. To expand the number of bits in the word: tie corresponding address pins together, tie write enable pins together, and bring data in and data out independently.
2. To expand the number of words: tie corresponding address pins together, tie write enable pins and corresponding data in and data out pins together, and use the higher order system addresses in conjunction with the chip enables to pick one row of packages.

100000256
100000401 THRU 100000415
100000421 THRU 100000440

Pin Configuration



1024-Bit Programmable Bipolar Read Only Memory

Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

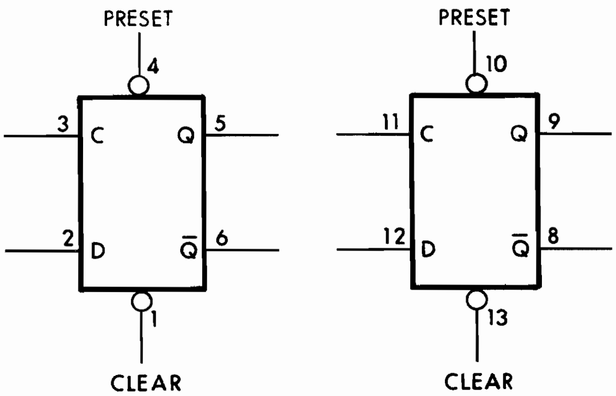
This integrated circuit is a high-speed, electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

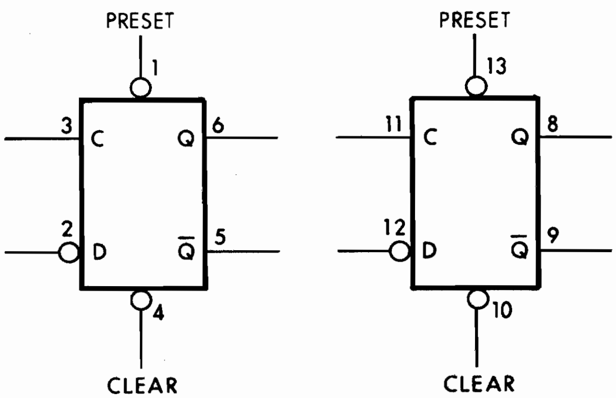
100000017 100000257 100000300

Dual D-Type Edge-Triggered Flip-Flop

Pin Connections



Alternate Pin Connections



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Function Table

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

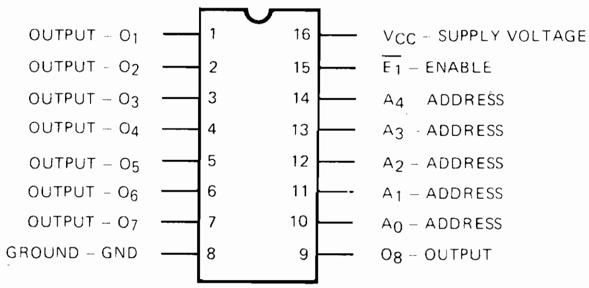
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Note: The 100000300 is a Schottky device.

REV. 03

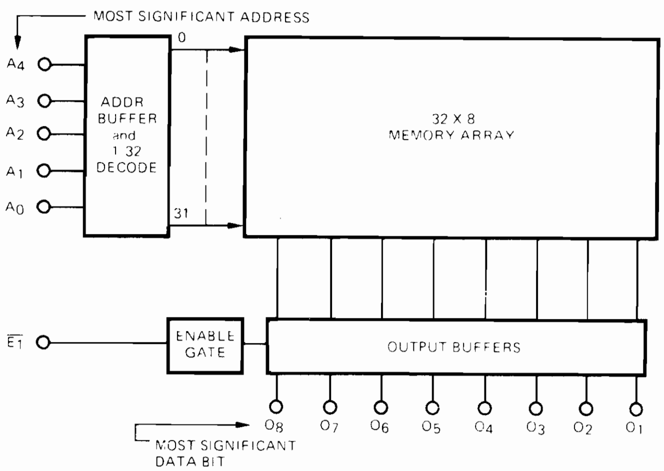
100000258 100000347 100000348 100000349 100000350 100000351 100000352 100000353 100000485 100000486

Pin Configuration



Low = Enable

Block Diagram



256 Bit Bipolar (32x8) Electrically Programmable Read Only Memory

This device is a field programmable, 256-bit, DTL and TTL compatible, bipolar read only memory.

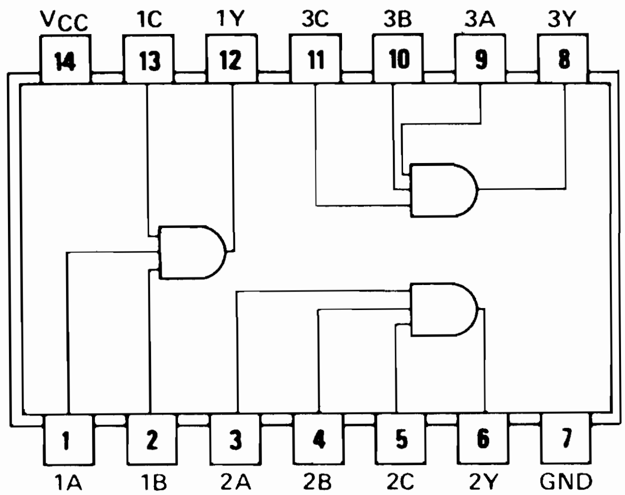
The three-state output of this device provides a low impedance driver Q_2 for driving capacitance on the memory output; no pullup resistor is required. When the chip enable is low, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. In a system enviornment, up to 21 memory outputs of the read only memory can be connected to a common bus. All of the devices, except one, are placed in the high impedance state. The selected device is enabled and has the characteristics of a TTL totem pole output.

Memory Operation

The memory is addressed with inputs A_0 through A_4 which select one of 32 words. To enable the outputs for a readout, enable E_1 must be low. If the enable is high, the outputs are held off permitting wire "OR"ing of the three-state outputs of several packages. The use of the enable permits expansion to greater than 32 words.

100000259

Pin Configuration



Triple 3-Input Positive-AND Gate With Open-Collector Outputs

Logic Diagram/Pin Designations

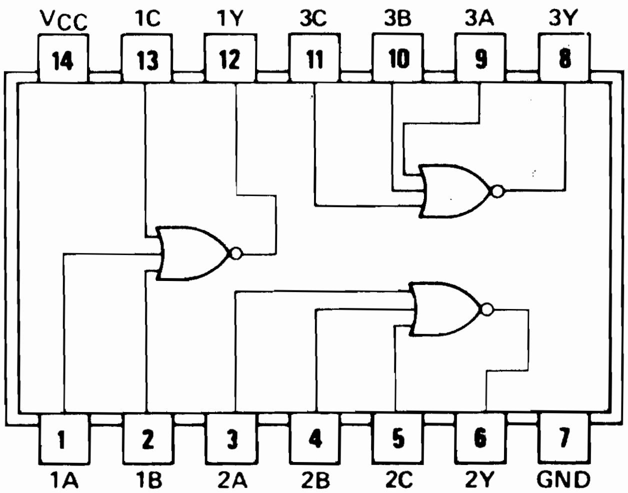
V_{CC} = Pin 14
Gnd = Pin 7

Positive logic: Y = ABC

Note: The 100000259 is a Schottky device.

100000260

Pin Configuration



Triple 3-Input Positive-NOR Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

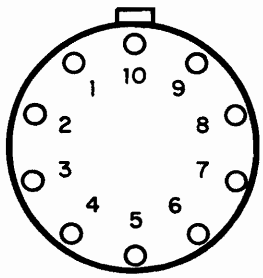
Gnd = Pin 7

Positive logic: $Y = \overline{A+B+C}$

100000261

Phase Locked Loop

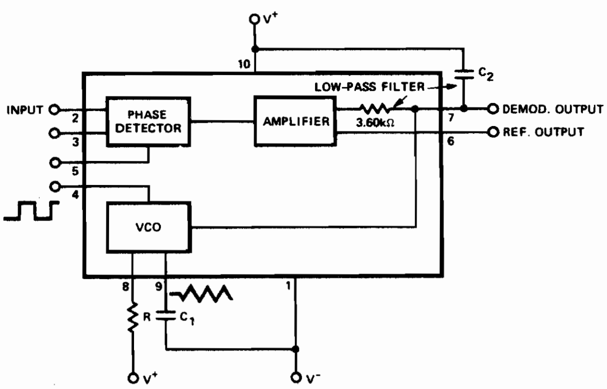
Pin Configuration



Pin Designations

1. V^-
2. Input
3. Input
4. VCO Output
5. Phase Comparator VCO Input
6. Reference Output
7. Demodulated Output
8. External R for VCO
9. External C for VCO
10. V^+

Functional Block Diagram

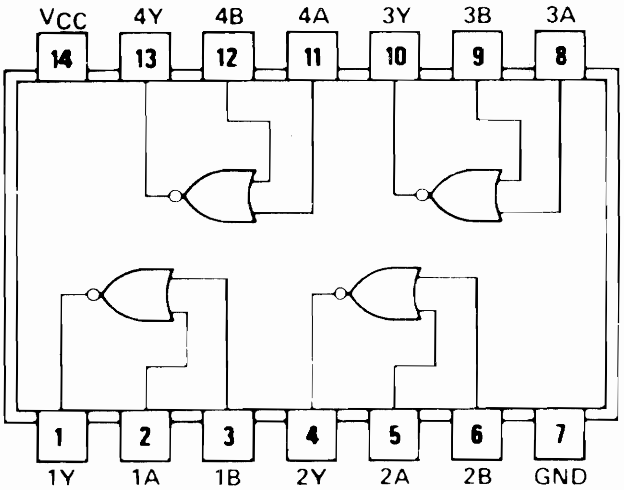


This Phase Locked Loop is a self-contained, adaptable filter and demodulator for the frequency range 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator, a phase comparator, an amplifier and a low-pass filter.

The center frequency of the device is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

100000262 100000330
100000341 100000366

Pin Configuration



Quadruple 2-Input Positive-NOR Gate

Logic Diagram/Pin Designations

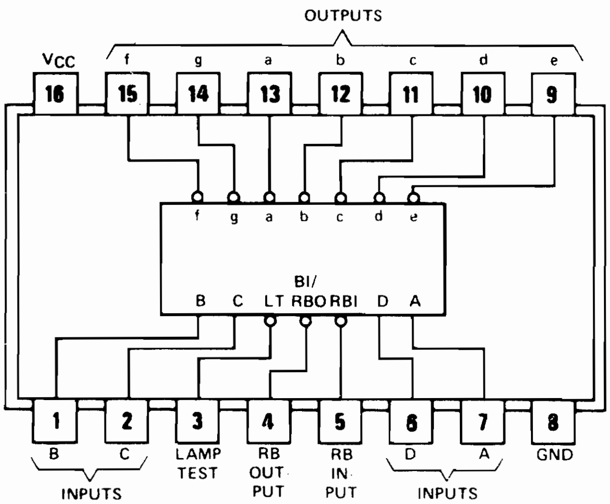
V_{CC} = Pin 14

Gnd = Pin 7

Positive logic: $Y = \overline{A+B}$

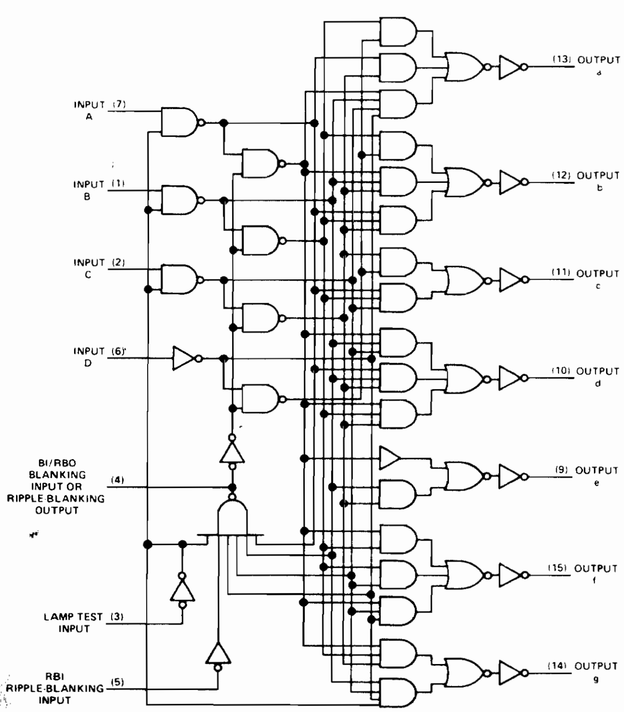
100000263

Pin Configuration



Positive Logic: See Function Table

Logic Diagram



BCD-To-Seven-Segment Decoder - Driver

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Function Table

Decimal or Function	Inputs						BI/RBO*	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	On	On	On	On	On	On	Off	1
1	H	X	L	L	L	H	H	Off	On	On	Off	Off	Off	Off	1
2	H	X	L	L	H	L	H	On	On	Off	On	On	Off	On	
3	H	X	L	L	H	H	H	On	On	On	On	Off	Off	On	
4	H	X	L	H	L	L	H	Off	On	On	Off	Off	On	On	
5	H	X	L	H	L	H	H	On	Off	On	On	Off	On	On	
6	H	X	L	H	H	L	H	Off	Off	On	On	On	On	On	
7	H	X	L	H	H	H	H	On	On	On	Off	Off	Off	Off	
8	H	X	H	L	L	L	H	On	On	On	On	On	On	On	
9	H	X	H	L	L	H	H	On	On	On	Off	Off	On	On	
10	H	X	H	L	H	L	H	Off	Off	Off	On	On	Off	On	
11	H	X	H	L	H	H	H	Off	Off	On	On	Off	Off	On	
12	H	X	H	H	L	L	H	Off	On	Off	Off	Off	On	On	
13	H	X	H	H	L	H	H	On	Off	Off	On	Off	On	On	
14	H	X	H	H	H	L	H	Off	Off	Off	On	On	On	On	
15	H	X	H	H	H	H	H	Off	Off	Off	Off	Off	Off	Off	
BI	X	X	X	X	X	X	L	Off	Off	Off	Off	Off	Off	Off	2
RBI	H	L	L	L	L	L	L	Off	Off	Off	Off	Off	Off	Off	3
LT	L	X	X	X	X	X	H	On	On	On	On	On	On	On	4

H = High level; L = Low level; X = irrelevant.

Notes:

1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.

3. When ripple-blanking input (RBI) and inputs A, B, C and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).

4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

* BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

Continued....

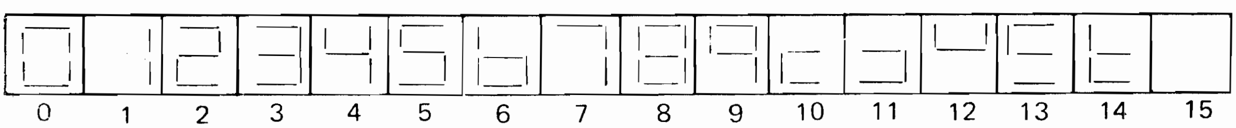
100000263

Continued

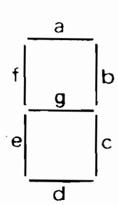
This circuit has full ripple-blanking input/output controls and a lamp test input. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

Automatic leading and/or trailing-edge zero-blanking control (RBI and RBO) is incorporated in this device. A lamp test (LT) may be performed at any time when the BI/RBO is at a high level. An overriding blanking input (BI) can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are compatible for use with TTL or DTL logic outputs.

Numerical Designations and Resultant Displays

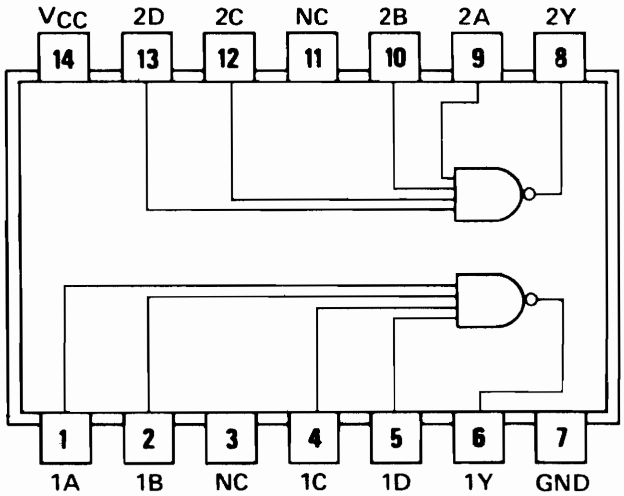


Segment Identification



100000264

Pin Configuration



Dual 4-Input Positive-NAND Buffer

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

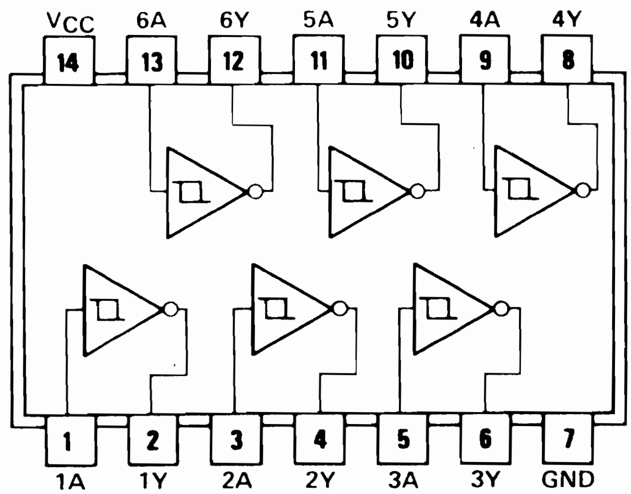
Positive logic: $Y = \overline{ABCD}$

Note: The 100000264 is a Schottky device.

100000265

Hex Schmitt-Trigger Inverter

Pin Configuration



Logic Diagram/Pin Designations

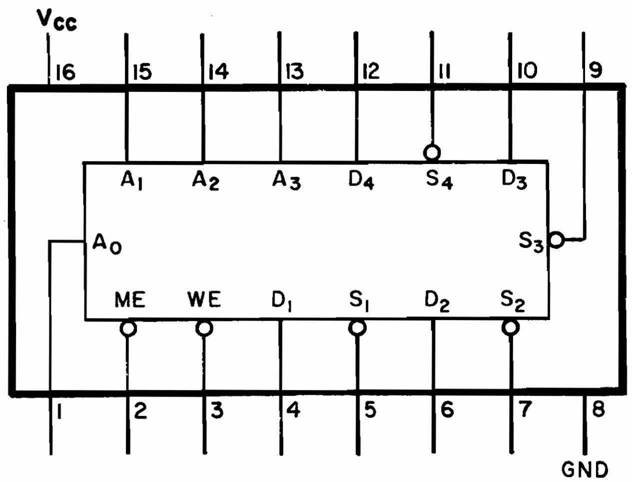
V_{CC} = Pin 14

Gnd = Pin 7

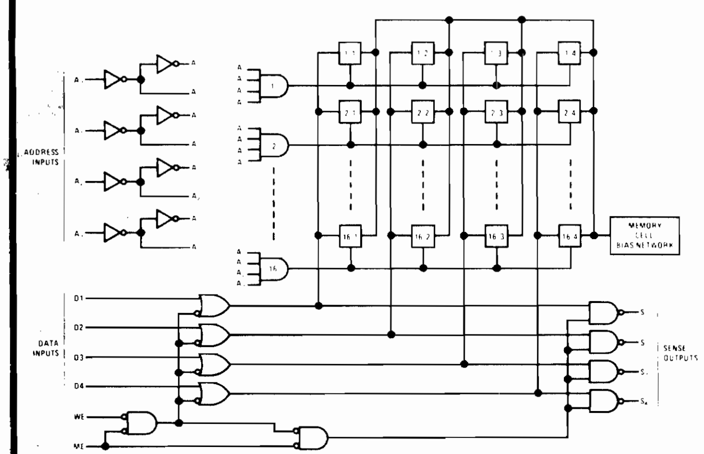
Positive logic: $Y = \overline{A}$

100000266

Pin Configuration



Functional Block Diagram



64-Bit Random Access Read/Write Memory

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

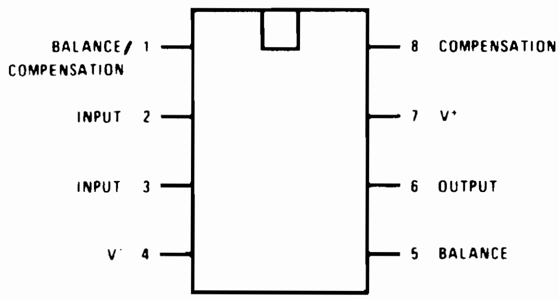
Truth Table

Memory Enable	Write Enable	Operation	Outputs
0	0	Write	Hi-Z State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Hi-Z State

The 100000266 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 128 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance while the one selected memory exhibits the normally totem-pole low impedance output characteristics of TTL.

100000267

Pin Configuration



Operational Amplifier

Pin Designations

V+ = Pin 7

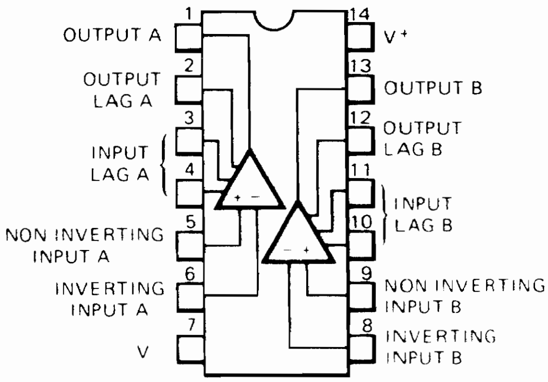
V- = Pin 4

The 100000267 is a general purpose operational amplifier. This amplifier offers overload protection on the input and output, no latch-up when the common mode range is exceeded, freedom from oscillations and compensation with a single 30pF capacitor.

In addition, the circuit can be used as a comparator with differential inputs up to ±30V, and the output can be clamped at any desired level to make it compatible with logic circuits.

100000268

Pin Configuration

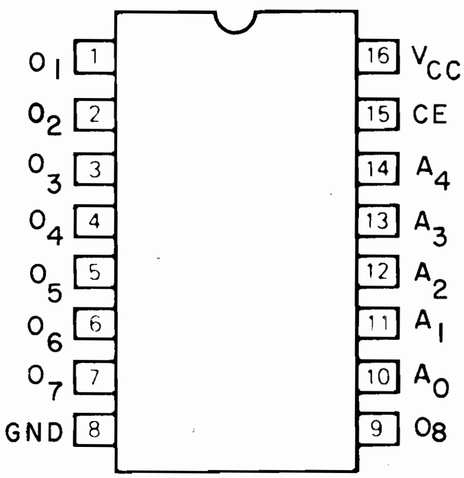


Dual Operational Amplifier

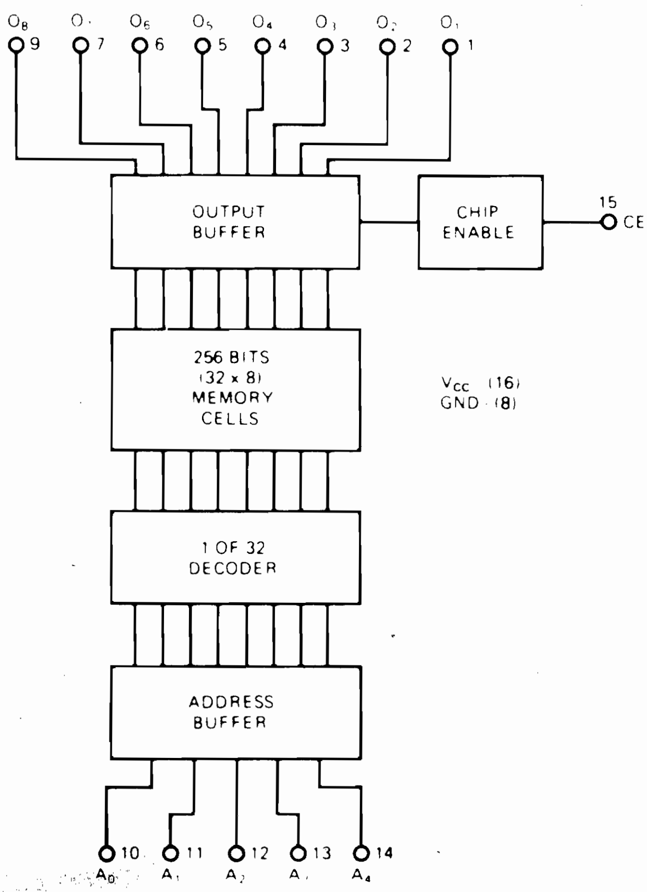
The 100000268 consists of two identical high gain operational amplifiers. These three-stage amplifiers use class A PNP transistor output stages with uncommitted collectors. The outputs may be ORed for use as a dual comparator or they may function as diodes in low threshold rectifying circuits.

100000140 100000141 100000142 100000148 100000149 100000215 100000216 100000217 100000218 100000219 100000269 100000270 100000271 100000272 100000273 100000274 100000275 100000276 100000277 100000278 100000279 100000280 100000499 100000500

Pin Configuration



Functional Block Diagram



256-Bit Bipolar Read Only Memory

Logic Diagram/Pin Designations

V_{CC} = Pin 16

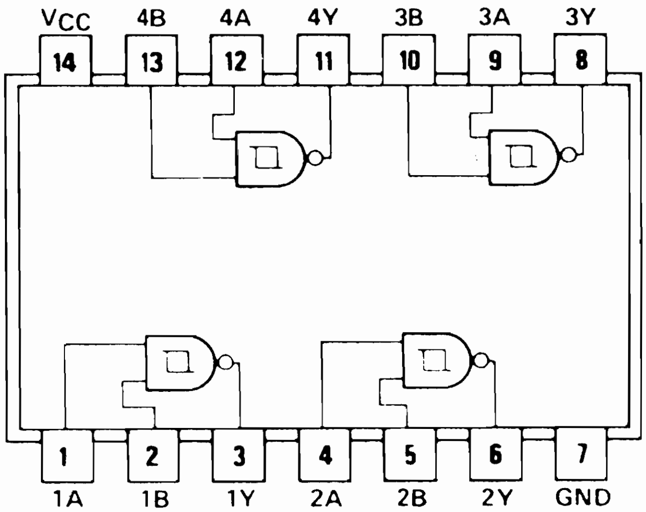
Gnd = Pin 8

These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

Memory expansion is simple; three-state outputs are provided on the 100000215; uncommitted collector outputs are provided on all other devices. Each device has on-chip address decoding and chip enable. The memory is fabricated with all logic level zeroes(low); logic level ones (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

100000281

Pin Configuration



Quadruple 2-Input Positive-NAND Schmitt Trigger

Logic Diagram/Pin Designations

V_{CC} = Pin 14

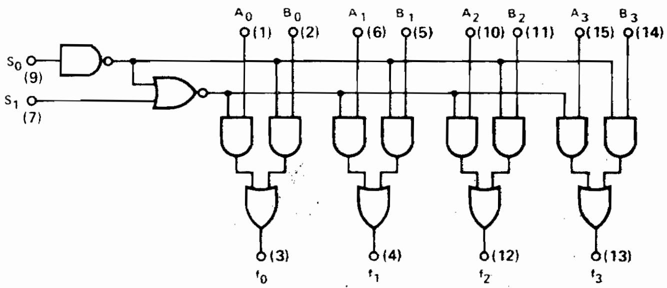
Gnd = Pin 7

Positive logic: $Y = \overline{AB}$

Note: The 100000281 is a Schottky device.

100000282

Logic Diagram



2-Input 4-Bit Digital Multiplexer

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Truth Table

S_0	S_1	f_n
0	0	B
1	0	A
0	1	B
1	1	0

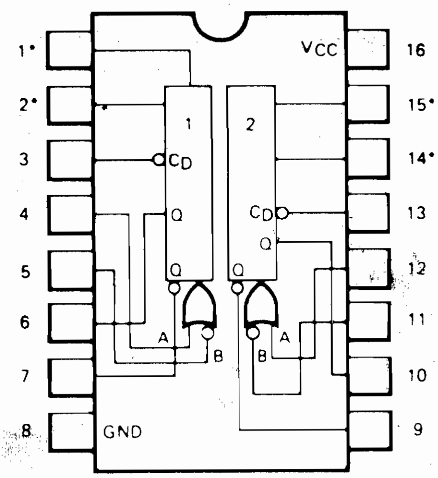
This 2-input, 4-bit digital multiplexer features non-inverting data paths.

The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

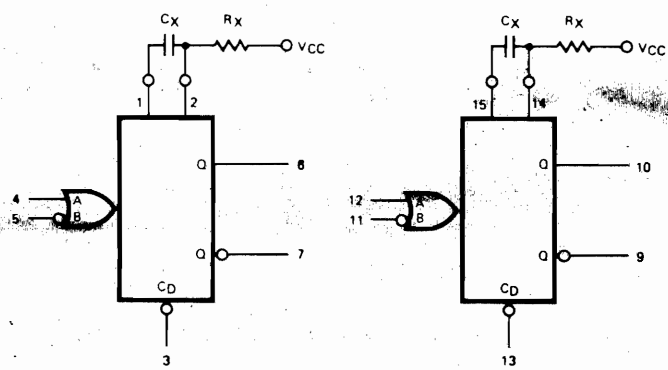
100000283

Low Power Dual Retriggerable Resettable Monostable Multivibrator

Pin Configuration



Functional Schematic



Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Triggering Truth Table

Pin Numbers			
5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

Notes:

H = High Voltage Level ≥ V_{IH}

L = Low Voltage Level ≤ V_{IL}

X = Don't Care (either H or L)

H→L = High to Low Voltage Level transition

L→H = Low to High Voltage Level transition

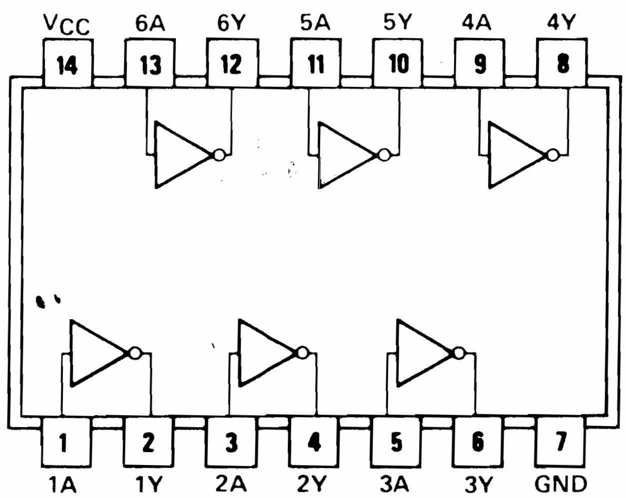
This dual resettable, retriggerable monostable multivibrator has two inputs per function, one active Low and one active High. This allows leading edge of trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger this device and result in a continuous true output.

The output pulse may be terminated at any time by connecting the reset pin to a logic level Low. Active pullups are provided on the outputs for good drive capability into capacitive loads.

Retriggering may be inhibited by tying the $\overline{Q}$ output to the active level Low input or the Q output to the active level High input.

100000188 100000284

Pin Configuration



Hex Inverter With Open-Collector Outputs

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

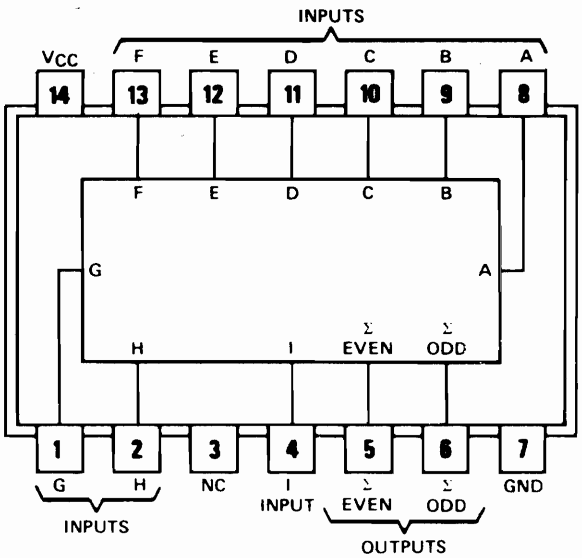
Positive logic: $Y = \overline{A}$

Note: The 100000188 is a Schottky device.

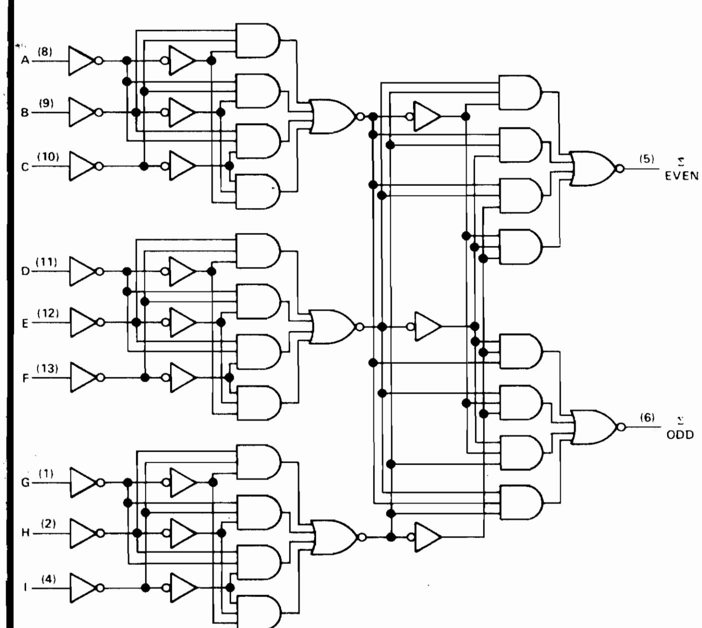
100000287

9-Bit Odd/Even Parity Generator/Checker

Pin Configuration



Logic Diagram



Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

NC = No internal connection

Function Table

Number of Inputs A Thru I That Are High	Outputs Σ Even	Outputs Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level
L = low level

This universal, monolithic, nine-bit parity generator/checker utilizes Schottky-clamped TTL circuitry and features odd/even outputs to facilitate operation of either odd or even parity applications. The word-length capability is expanded by cascading.

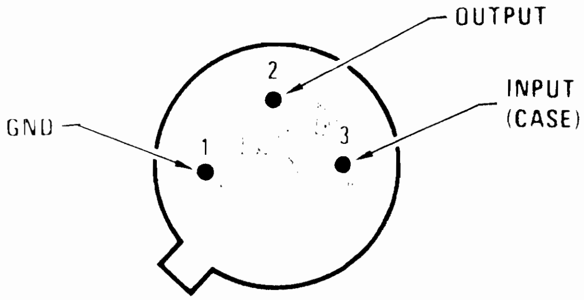
100000290 100000354 100000379

Three-Terminal Negative Regulator

The 100000290, 100000354, and the 100000379 are three-terminal negative regulators. The 100000290 and the 100000354 have fixed output voltages of -12V and the 100000379 has a fixed output voltage of -5V. These devices need only one external component--a compensation capacitor at the output.

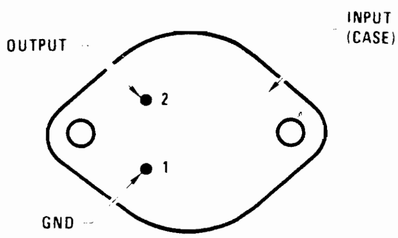
Pin Configuration

3-Lead Metal Box



BOTTOM VIEW

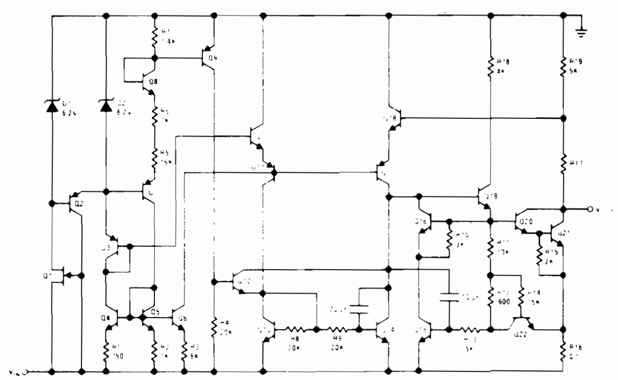
100000290



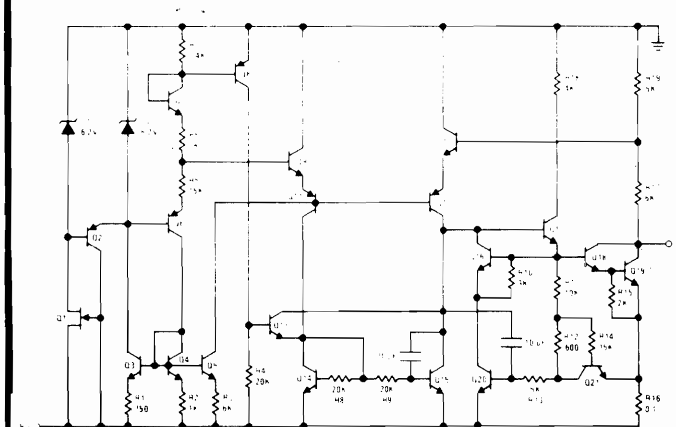
BOTTOM VIEW

100000354, 100000379

Schematic



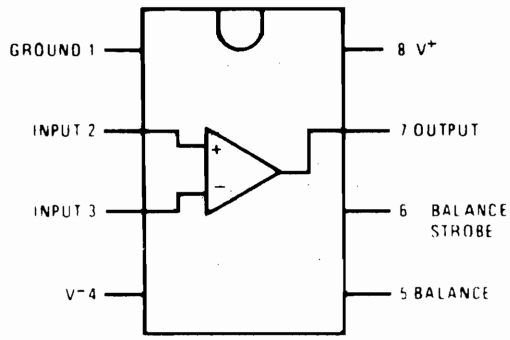
100000290, 100000354



100000379

100000292

Pin Configuration



Voltage Comparator/Buffer

Pin Designations

V+ = Pin 8

V- = Pin 4

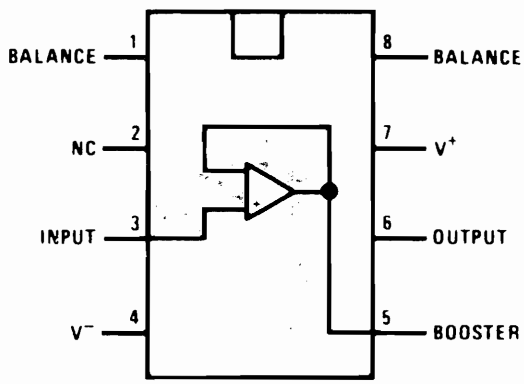
Gnd = Pin 1

This voltage comparator is designed to operate over a wide range of supply voltages. Its output is compatible with RTL, DTL and TTL as well as MOS circuits.

Both the input and output can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'd.

100000293

Pin Configuration



Operational Amplifier

Pin Designations

V+ = Pin 7

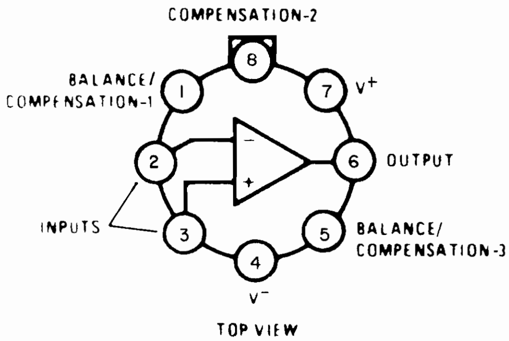
V− = Pin 4

The 100000293 is a monolithic operational amplifier internally connected as a unity-gain non-inverting amplifier. The device has internal frequency compensation and provision for offset balancing.

100000294

Pin Configuration

Metal Can Package



Operational Amplifier

Pin Designations

V+ = Pin 7

V- = Pin 4

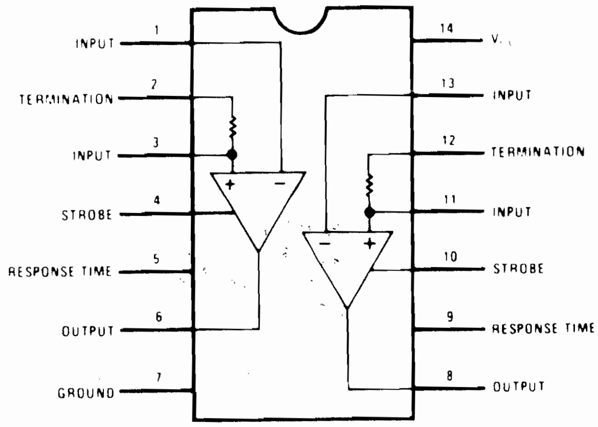
This precision high-speed operational amplifier has internal unity gain frequency compensation, which simplifies its application since no external components are necessary for operation. However, external frequency compensation may be added for optimum performance.

For inverting applications, feed-forward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. A single capacitor can be added to reduce the 0.1% settling time to under 1μs.

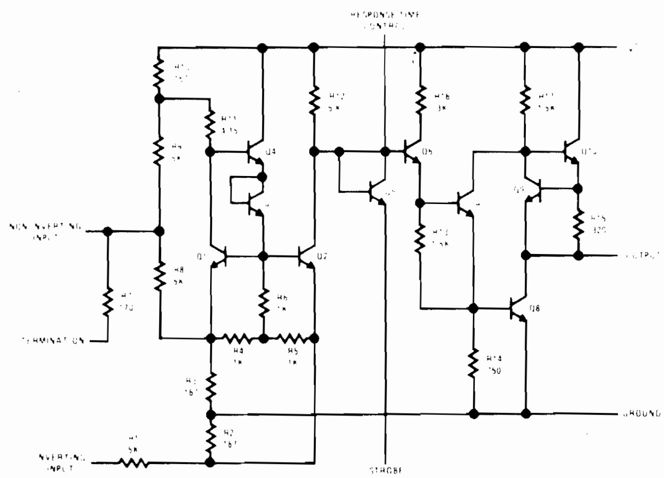
100000295

Dual Line Receiver

Pin Configuration



Schematic



Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

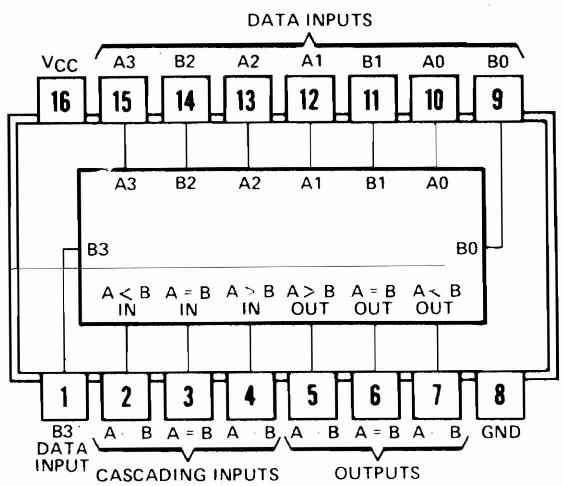
The 100000295 is a digital line receiver. The response time can be controlled with an external capacitor to eliminate noise spikes. The output is directly compatible with RTL, DTL or TTL integrated circuits.

REV. 03

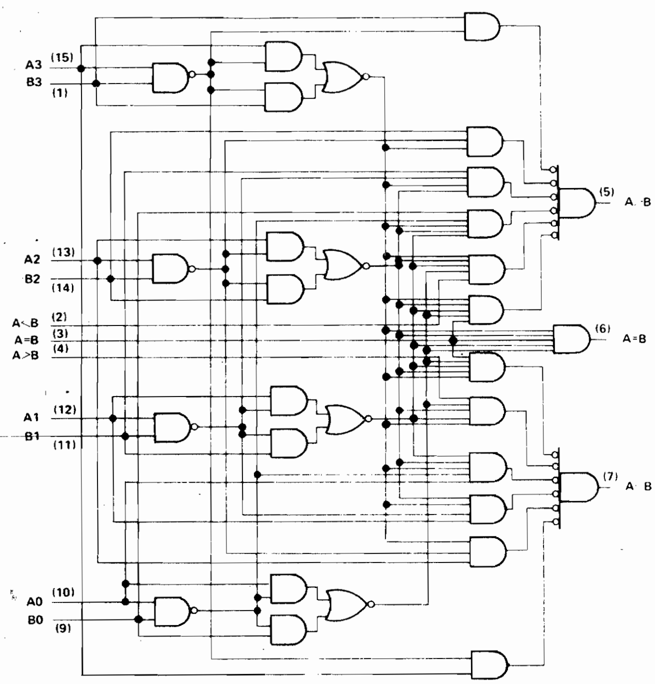
100000296

4-Bit Magnitude Comparator

Pin Configuration



Logic Diagram



Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B2	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H = high level
L = low level
X = irrelevant

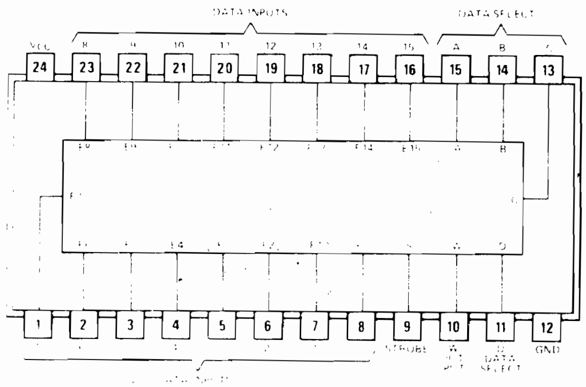
This four-bit magnitude comparator performs comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions for two 4-bit words (A, B) are made and are externally available at three outputs. This device is fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A>B, A<B, and A=B outputs of a stage handling less-significant bits are connected to the corresponding A>B, A<B, and A=B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A=B input.

Note: The 100000296 is a Schottky device.

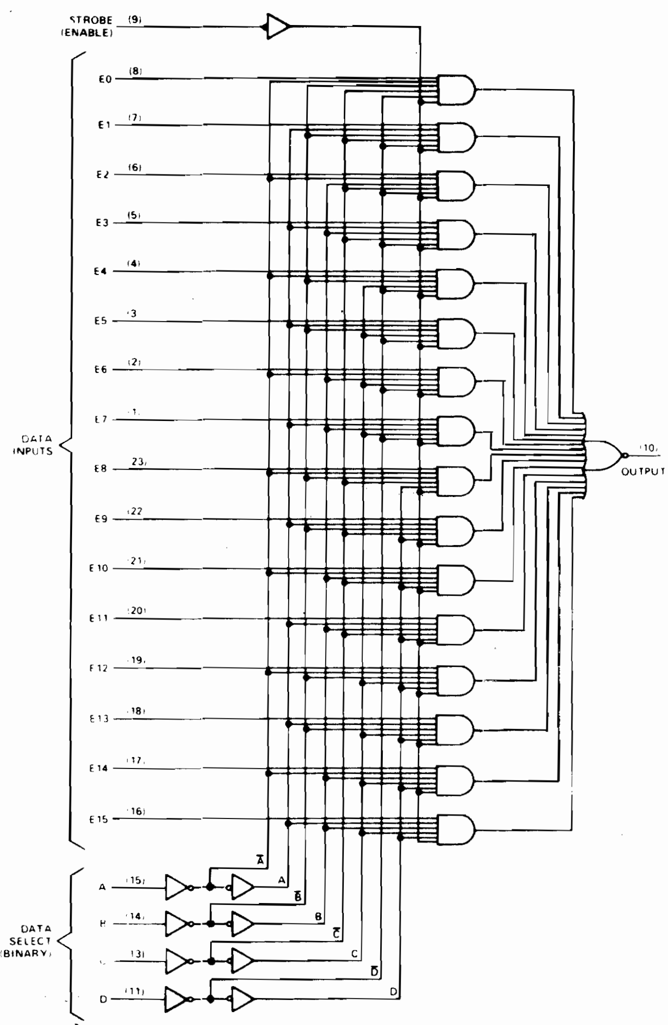
100000297

Data Selector/Multiplexer

Pin Configuration



Logic Diagram



Pin Designations

V_{CC} = Pin 24

Gnd = Pin 12

Function Table

Inputs		Output
Select D C B A	Strobe S	W
X X X X	H	H
L L L L	L	$\overline{E0}$
L L L H	L	$\overline{E1}$
L L H L	L	$\overline{E2}$
L L H H	L	$\overline{E3}$
L H L L	L	$\overline{E4}$
L H L H	L	$\overline{E5}$
L H H L	L	$\overline{E6}$
L H H H	L	$\overline{E7}$
H L L L	L	$\overline{E8}$
H L L H	L	$\overline{E9}$
H L H L	L	$\overline{E10}$
H L H H	L	$\overline{E11}$
H H L L	L	$\overline{E12}$
H H L H	L	$\overline{E13}$
H H H L	L	$\overline{E14}$
H H H H	L	$\overline{E15}$

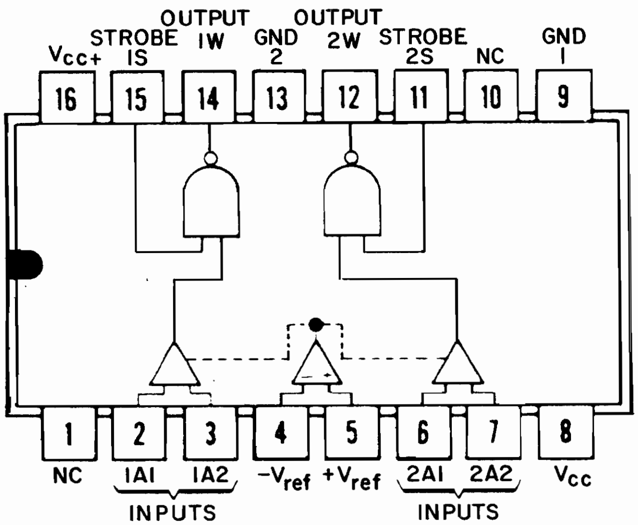
H = high level, L = low level, X = irrelevant.

$\overline{E0}$, $\overline{E1}$ .... $\overline{E15}$ = the complement of the level of the respective E input.

This monolithic data selector/multiplexer contains full on-chip binary decoding to select one-of-sixteen data sources. The strobe input must be at a low logic level to enable this device. A high level at the strobe forces the W output high and the Y output low. The 100000297 has an inverted (W) output only.

100000118 100000229
100000298 100000299

Pin Configuration



Dual Sense Amplifiers

Logic Diagram/Pin Designations

V_{CC+} = Pin 16

V_{CC} = Pin 8

Gnd 1 = Pin 9

Gnd 2 = Pin 13

NC = No internal connection

Positive logic: $W = \overline{AS}$

Truth Table

Inputs A	Inputs S	Output W
H	H	L
L	X	H
X	L	H

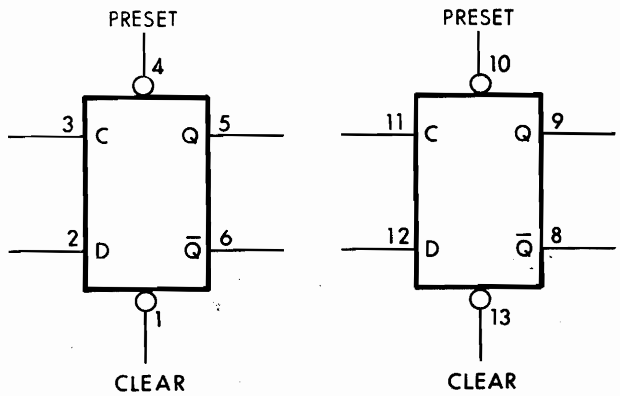
Definition of logic levels:

Input	H	L	X
A*	$V_{ID} \geqslant V_{Tmax}$	$V_{ID} \leqslant V_{Tmin}$	Irrelevant
S	$V_I \geqslant V_{IHmin}$	$V_I < V_{ILmax}$	Irrelevant

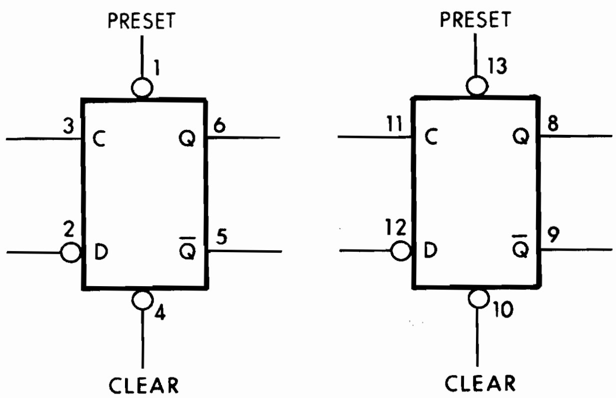
* A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

100000017 100000257 100000300

Pin Connections



Alternate Pin Connections



Dual D-Type Edge-Triggered Flip-Flop

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Function Table

Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

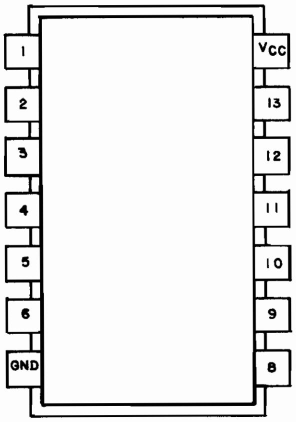
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Note: The 100000300 is a Schottky device.

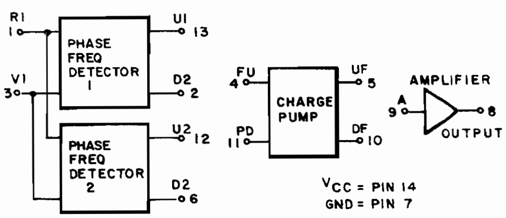
REV. 03

100000301

Pin Configuration



Schematic



INPUT LOADING FACTOR: RI, VI = 3
OUTPUT LOADING FACTOR (PIN 8) = 10
TOTAL POWER DISSIPATION = 85 mW TYP/PKG
PROPAGATION DELAY TIME = 9.0 ns TYP
(THRU PHASE DETECTOR)

Phase-Frequency Detector

Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

INPUT	INPUT		OUTPUT			
STATE	RI	VI	U1	D1	U2	D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	X	X	1	1
8	1	0	X	X	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

1. X indicates output state unknown
2. U1 and D1 outputs are sequential: i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational: i.e., they need only inputs shown to obtain outputs.

TRUTH TABLE

This is not strictly a functional truth table: i.e., it does not show all possible modes of operation. It is useful for dc testing.

Continued....

100000301

Continued

The 100000301 contains two digital phase detectors and a charge pump circuit which converts MTTL inputs to a dc voltage level for use in frequency discrimination and phase-locked loop applications.

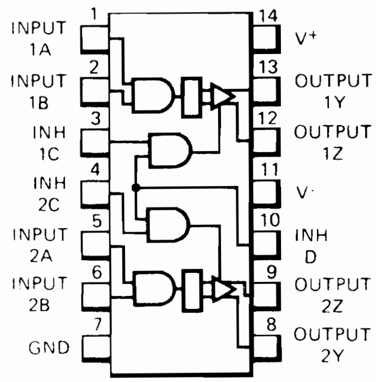
The two phase setectors have common inputs. Phase-frequency detector 1 is locked in (indicated by both outputs high) when the negative transitions of the variable input (VI) and reference input (RI) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, the U1 (up) output goes low; conversely the D1 (down) output goes low when the variable input is higher in frequency or leads the reference input in phase. It is important to note that the duty cycles of the variable input and the reference input are not important since negative transitions control system operation.

Phase detector 2, on the other hand, is locked in when the variable input phase lags the reference phase by 90° (indicated by the U2 and D2 outputs alternately going low with equal pulse widths). If the variable input phase lags by more than 90°, U2 will remain low longer than D2, and conversely, if the variable input phase lags the reference phase by less than 90°, D2 remains low longer. In this phase detector the variable input and the reference must have 50% duty cycles.

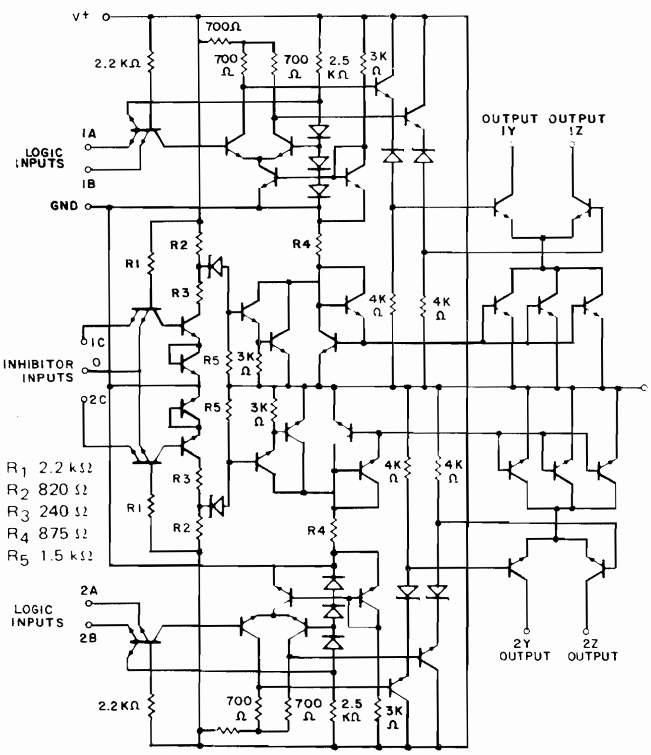
The charge pump accepts the phase detector outputs (U1 or U2 applied to PU, and D1 or D2 applied to PD) and converts them to fixed amplitude positive and negative pulses at the UF and DF outputs respectively. These pulses are applied to a lag-lead active filter, which incorporates external components, as well as the amplifier provided in the 100000301 circuit. The filter provides a dc voltage proportional to the phase error.

100000304

Pin Configuration



Schematic



Dual Line Driver

Pin Designations

V+ = Pin 14

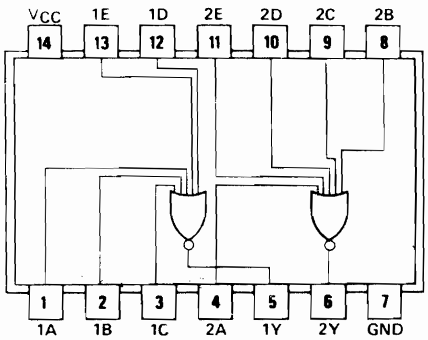
V- = Pin 11

Gnd = Pin 7

The 100000304 is a Dual Line Driver featuring independent channels with common supply voltage and ground terminals. The output current is nominally 12mA. The driver circuits have a constant output that is switched to either of two output terminals by the appropriate logic levels at the terminals. The output current can be switched off by appropriate logic levels at the input terminals. The circuit also features an inhibit input that is common to both drivers. The common-mode voltage range of the driver outputs is -3V to +10V, which allows a common-mode voltage on the line without affecting the driver performance.

100000305

Pin Configuration



Dual 5—Input Positive-NOR Gate

Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

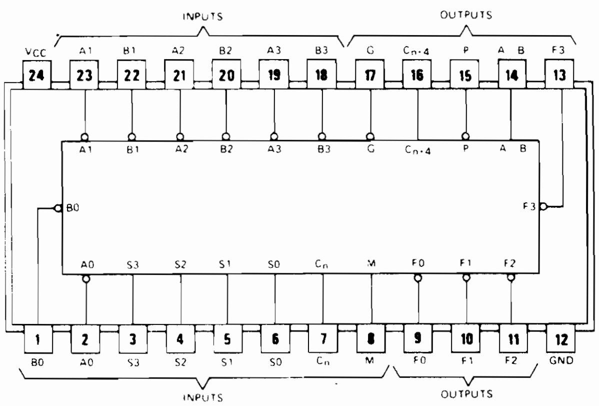
Positive logic: $\overline{Y=A+B+C+D+E}$

REV. 03

100000084 100000169 100000306

Arithmetic Logic Units/Function Generators

Pin Configuration



Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A=B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
Gnd	12	Ground

These arithmetic logic units (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip, and perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with 100000100 or 100000170, full carry look-ahead circuits, high-speed arithmetic operations can be performed. If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay is minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These devices will accommodate active-high or active-low data if the pin designations are interpreted as follows:

Continued.....

100000084 100000169 100000306

Continued

Table 1

Selection S3 S2 S1 S0	M = H Logic Functions	Active-High Data M = L: Arithmetic Operations C_n = H (no carry)	C_n = L (with carry)
L L L L	F = $\overline{A}$	F = A	F = A Plus 1
L L L H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L L H L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L L H H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L H L L	F = $\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L H L H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L H H L	F = A$\oplus$B	F = A Minus B Minus 1	F = A Minus B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H L L H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H L H H	F = AB	F = AB Minus 1	F = AB
H H L L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H H L H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H H H L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H H H H	F = A	F = A Minus 1	F = A

* Each bit is shifted to the next more significant position.

Table 2

Selection S3 S2 S1 S0	M = H Logic Functions	Active-Low Data M = L: Arithmetic Operations C_n = L (no carry)	C_n = H (with carry)
L L L L	F = $\overline{A}$	F = A Minus 1	F = A
L L L H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L L H L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L L H H	F = 1	F = Minus 1 (2's Comp)	F = Zero
L H L L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L H L H	F = $\overline{B}$	F = AB Plus (A + $\overline{B}$)	F = AB Plus (A + $\overline{B}$) Plus 1
L H H L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L H H H	F = A + B	F = A + B	F = (A + $\overline{B}$) Plus 1
H L L L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H L L H	F = A$\oplus$B	F = A Plus B	F = A Plus B Plus 1
H L H L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H L H H	F = A + B	F = A + B	F = (A + B) Plus 1
H H L L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H H L H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H H H L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H H H H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.

Pin No.	Active-high data Table 1	Active-low data Table 2
2	A_0	$\overline{A}_0$
1	B_0	$\overline{B}_0$
23	A_1	$\overline{A}_1$
22	B_1	$\overline{B}_1$
21	A_2	$\overline{A}_2$
20	B_2	$\overline{B}_2$
19	A_3	$\overline{A}_3$
18	B_3	$\overline{B}_3$
9	F_0	$\overline{F}_0$
10	F_1	$\overline{F}_1$
11	F_2	$\overline{F}_2$
13	F_3	$\overline{F}_3$
7	$\overline{C}_n$	C_n
16	$\overline{C}_{n+4}$	C_{n+4}
15	X	$\overline{P}$
17	Y	$\overline{G}$

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

These devices can also be utilized as comparators. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

Input C_n	Output C_{n+4}	(Figure 1) Active-high Data	(Figure 2) Active-low Data
H	H	$A \leqslant B$	$A \geqslant B$
H	L	$A > B$	$A < B$
L	H	$A < B$	$A > B$
L	L	$A \geqslant B$	$A \leqslant B$

Continued....

100000084 100000169 100000306

Continued

Figure 1

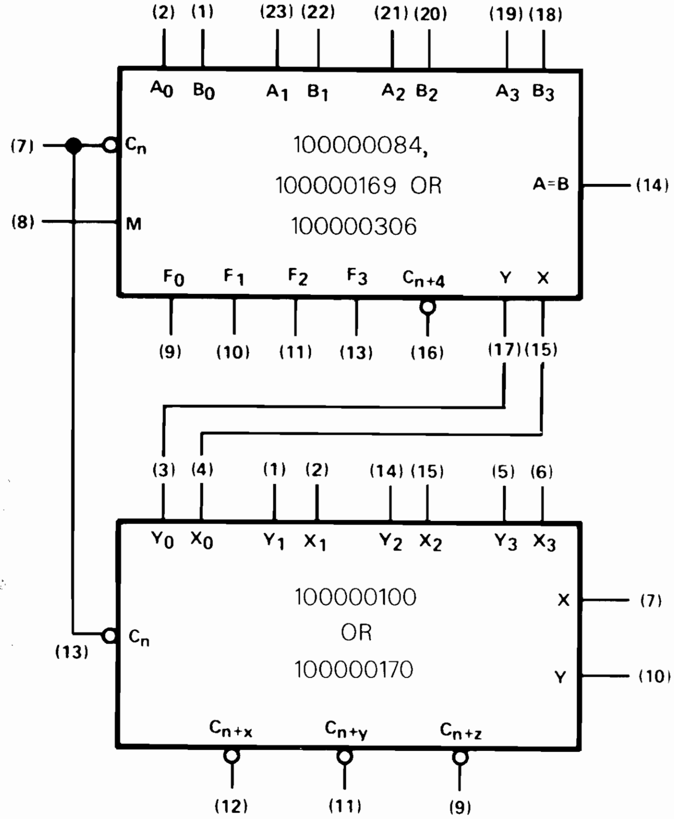
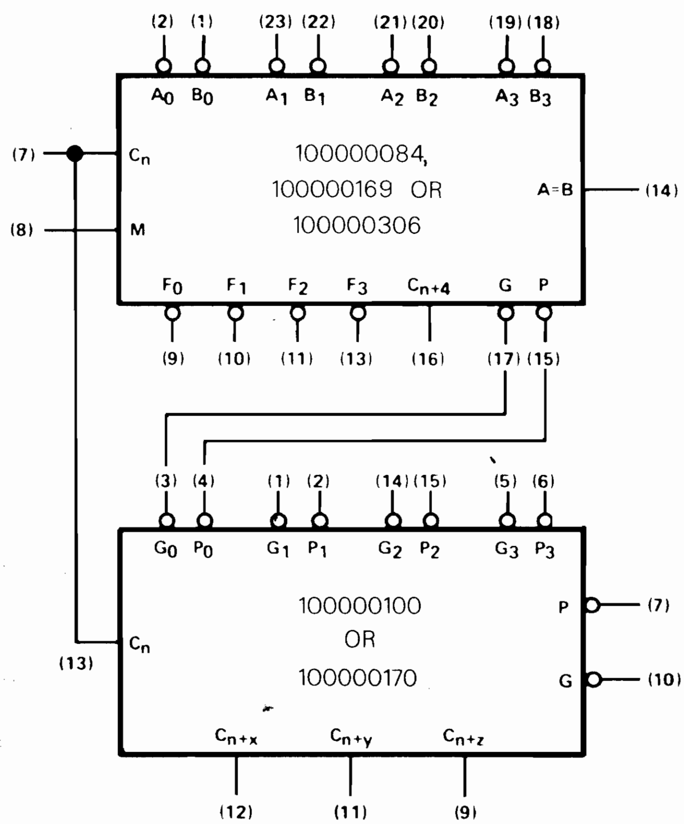


Figure 2



These circuits have been designed to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR and OR functions.

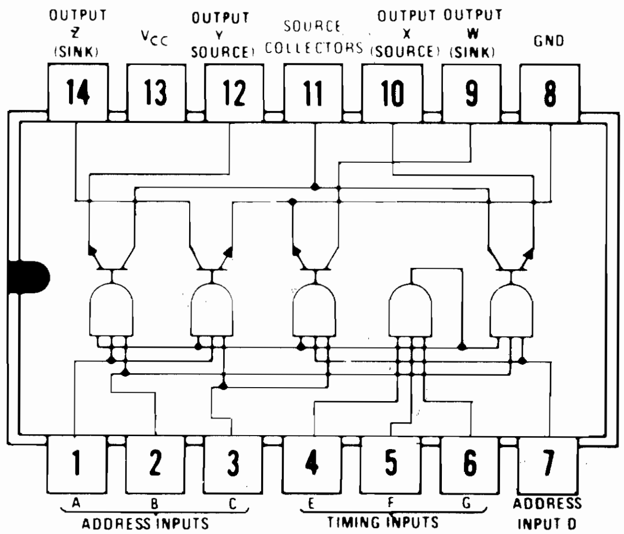
ALU Signal Designations

These devices can be used with the signal designations of either Figure 1 or Figure 2. The logic functions and arithmetic operations obtained with the signal designations of Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

Note: The 100000169 is a Schottky device.

100000079 | 100000307

Pin Configuration



Memory Driver with Decode Inputs

Logic Diagram/Pin Designations

V_{CC} = Pin 13

Gnd = Pin 8

Truth Table

Inputs							Outputs			
Address				Timing			Sink	Sources		Sink
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	On	Off	Off	Off
0	1	0	1	1	1	1	Off	On	Off	Off
1	1	0	0	1	1	1	Off	Off	On	Off
1	0	1	0	1	1	1	Off	Off	Off	On
X	X	X	X	0	X	X	Off	Off	Off	Off
X	X	X	X	X	0	X	Off	Off	Off	Off
X	X	X	X	X	X	0	Off	Off	Off	Off

Notes:

X = Logical 1 or logical 0.

Not more than one output is allowed to be On at one time: When all timing inputs are at a logical 1, two of the address inputs must be at a logical 0.

This monolithic memory driver with decode inputs is designed for use with magnetic memories. The device contains two 400 milliampere (source/sink) switch pairs, with decoding capability from four address lines. Two address inputs (B and C) are used for mode selection; i.e., source or sink. The other two address inputs (A and D) are used for switch-pair selection; i.e., output switch-pair Y/Z or W/X, respectively.

100000309 100000363

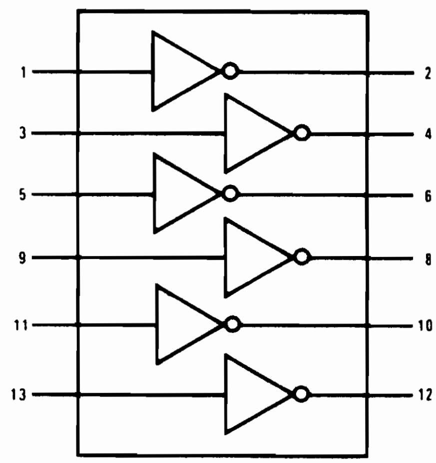
Hex Inverter

Pin Designations

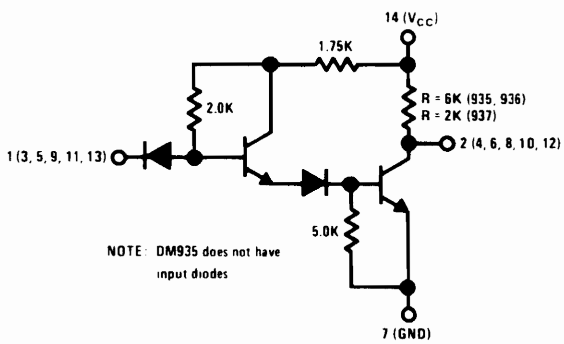
V_{CC} = Pin 14

Gnd = Pin 7

Connection/Logic Diagram



Schematic Diagram



100000310

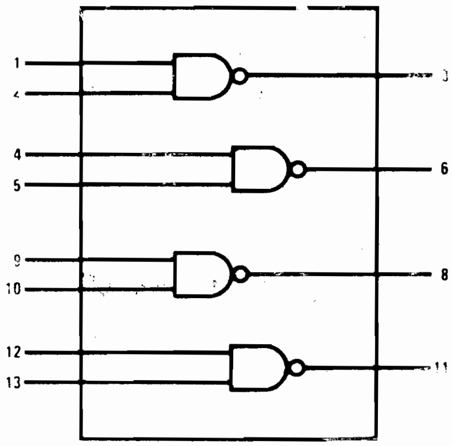
Quad 2-Input NAND Gate

Pin Designations

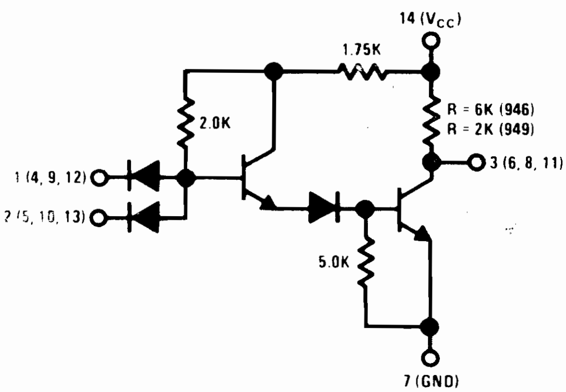
V_{CC} = Pin 14

Gnd = Pin 7

Connection/Logic Diagram



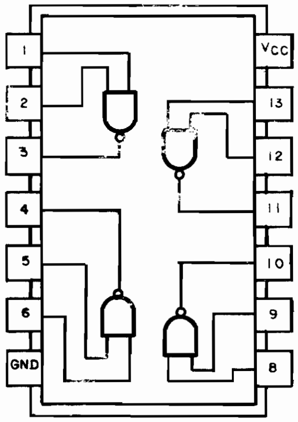
Schematic Diagram



100000311

Quadruple 2-Input NAND Power Gate

Pin Configuration



Pin Designations

V_{CC} = Pin 14

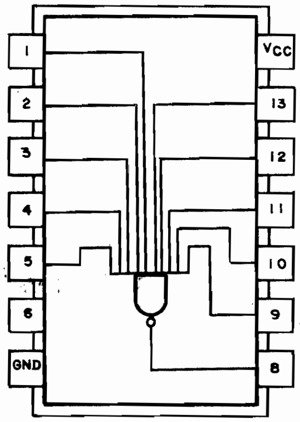
Gnd = Pin 7

REV. 03

100000312

10 Input NAND Gate

Pin Configuration



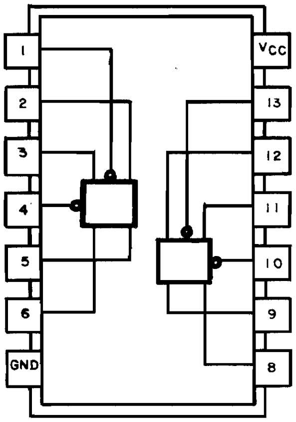
Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

100000313

Pin Configuration



Dual J-K Flip-Flop with Individual Clocks and Presets

Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

TRUTH TABLE 5

t_n		t_n+1
J	K	Q
L	L	Qn
H	H	H
H	H	$\overline{Q}n$

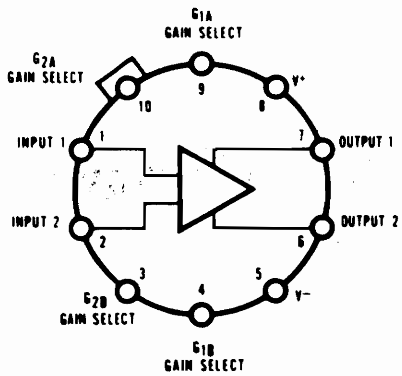
100000062 100000314
100000326 100000372

Differential Video Amplifier

This device is a monolithic two-stage differential input, differential output video amplifier. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. This device provides fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option.

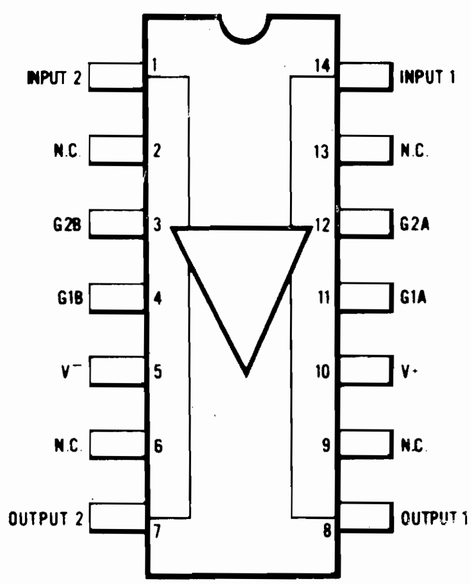
Pin Configuration

Top View



100000062, 100000326

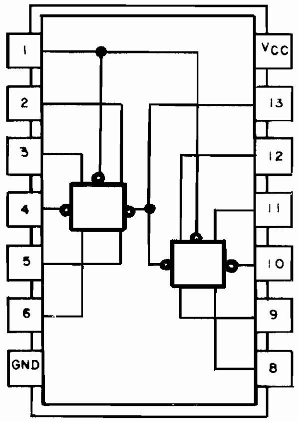
TO-116 DUAL IN-LINE



100000314, 100000372

100000316

Pin Configuration



Dual J-K Flip-Flop with Common Clocks and Clears

Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

TRUTH TABLE 5

t_n		t_n+1
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Q}$n

REV. 03

100000317 100000334

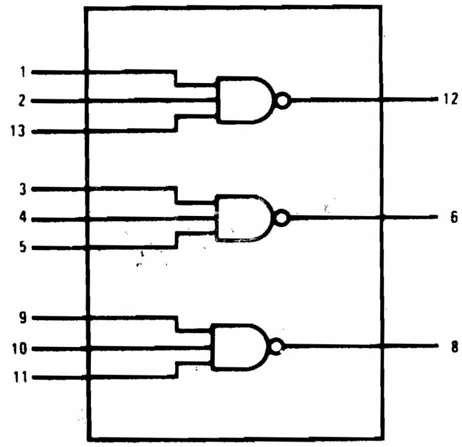
Triple Three Input NAND Gate

Pin Designations

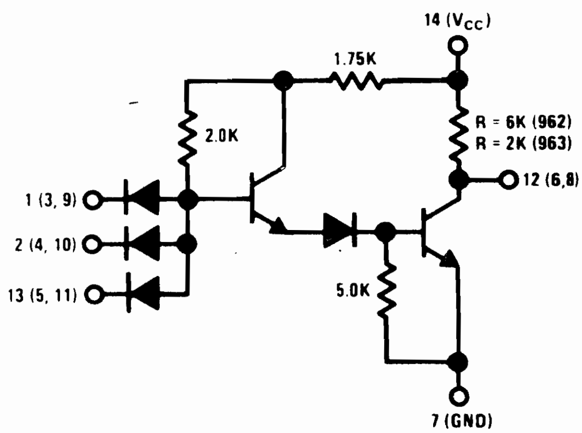
V_{CC} = Pin 14

Gnd = Pin 7

Connection/Logic Diagram



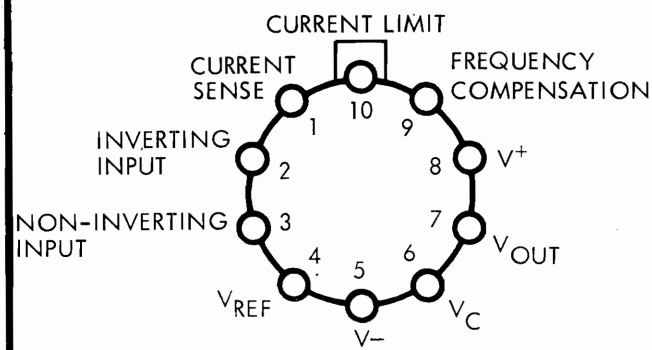
Schematic Diagram



REV. 03

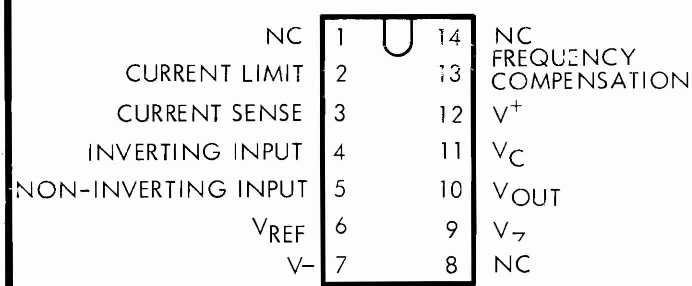
100000026 10000094 100000318

Pin Configurations



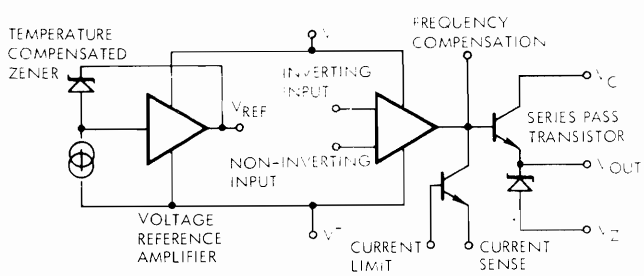
Note: pin 5 is connected to case

100000026



100000094

Equivalent Circuit



Precision Voltage Regulator

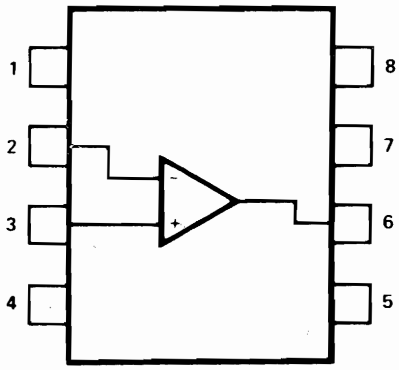
The 100000026(Can) and 100000094, 100000318(DIP) are monolithic voltage regulators, consisting of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150mA are required. Provisions are made for adjustable current limiting and remote shutdown.

REV. 03

100000156 100000319

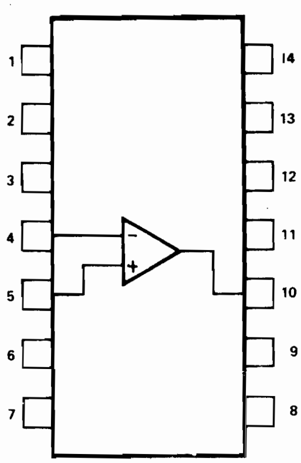
Pin Configuration

100000156



(Top View)

100000319



High Performance Operational Amplifier

Pin Designations

1. Offset Null
2. Inv. Input
3. Non-Inv. Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. NC

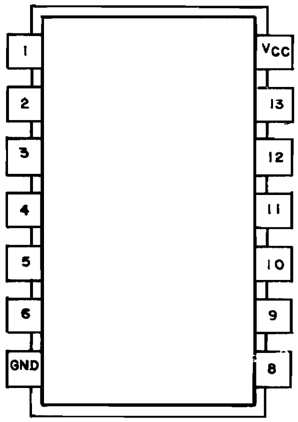
This device is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and temperature stability.

The device is short-circuit protected and allows for nulling of offset voltage.

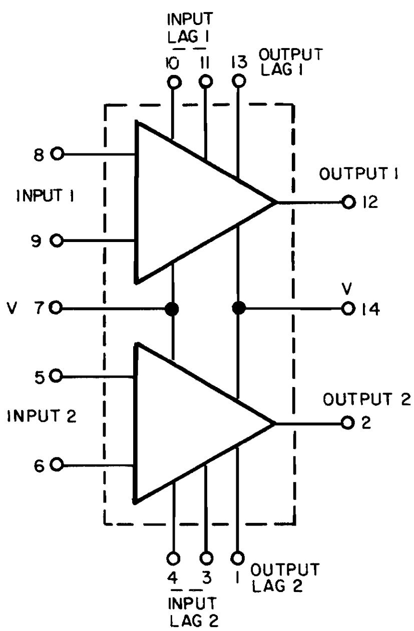
100000320

Monolithic Dual Operational Amplifier

Pin Configuration



Equivalent Circuit



Pin Designations

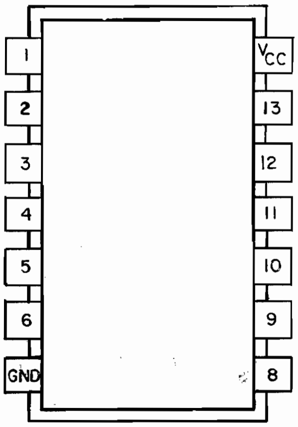
V_{CC} = Pin 14

Gnd = Pin 7

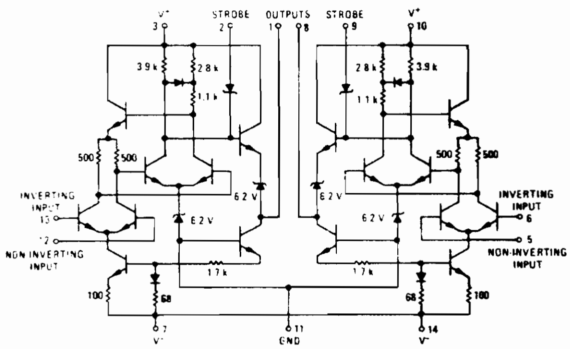
REV. 03

100000322

Pin Configuration



Circuit Schematic



Dual Differential Comparator

Pin Designations

V+ = Pin 3 and Pin 10

V- = Pin 7 and Pin 14

Gnd = Pin 11

REV. 03

100000323

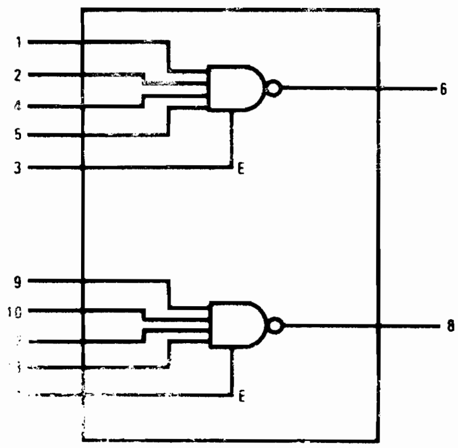
Dual 4-Input NAND Power Gate with Expander

Pin Designations

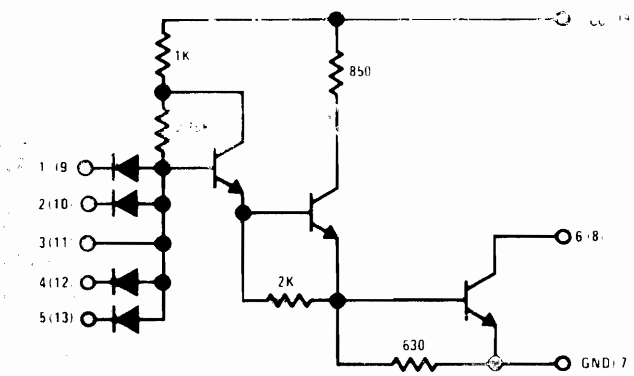
V_{CC} = Pin 14

Gnd = Pin 7

Connection/Logic Diagram



Schematic Diagram



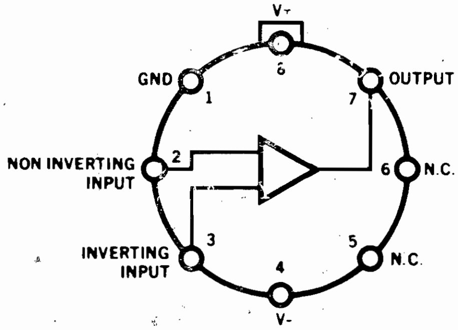
DM944

100000059 100000157 100000324

High-Speed Differential Comparator

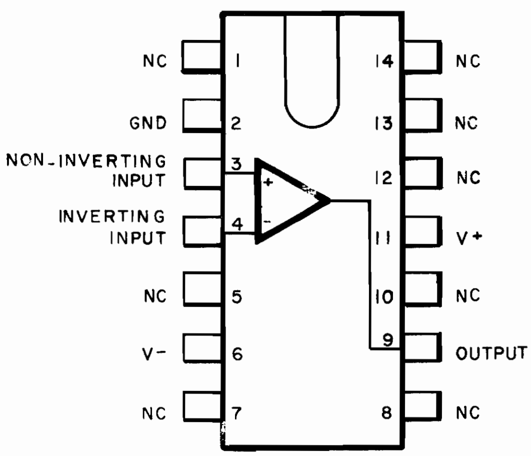
Pin Configurations

100000059, 100000324



Note: Pin 4 connected to case.

100000157



The 100000059 & 100000324 (can) and 100000157 (DIP) are differential voltage comparators intended for applications requiring high accuracy fast response times. Constructed on a single silicon chip, the devices are useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high-noise immunity line receiver.

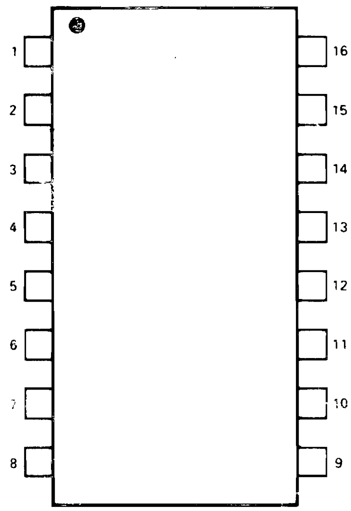
100000325

Dual Differential Amplifier

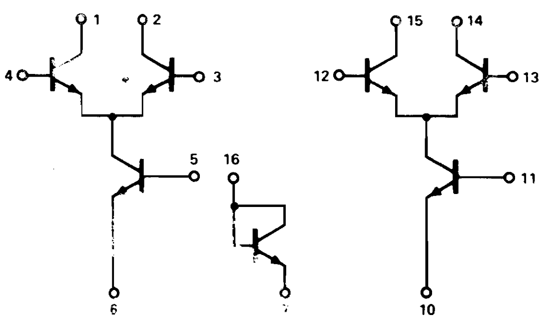
The 100000325 is a monolithic dual high frequency differential amplifier with associated constant current source transistors and biasing diode. It is useful from DC to 100 MHz. The circuit arrangement provides for connection as two completely independent emitter coupled (differential) or cascode amplifiers. The bias diode allows stabilization of the current source currents over a large temperature range.

Pin Configuration

(Top View)



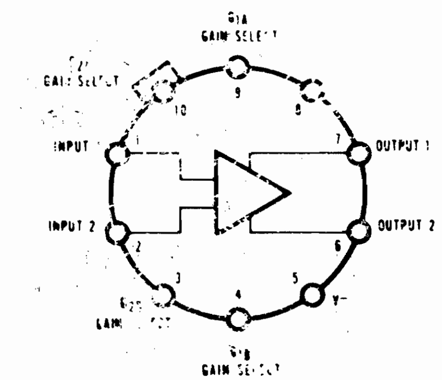
Basic Circuit Schematic



REV. 03

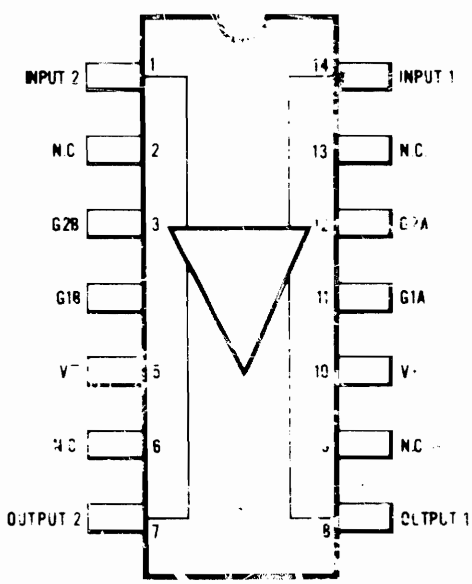
100000062 100000326 | 100000314 100000372

Pin Configuration
Top View



100000062, 100000326

TO-116 DUAL IN-LINE



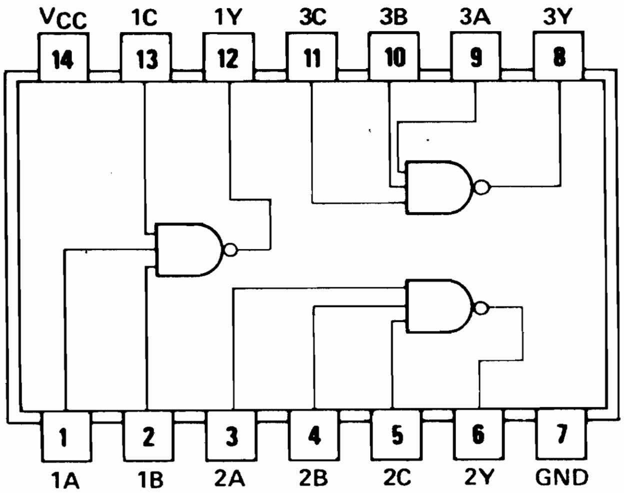
100000314 100000372

Differential Video Amplifier

This device is a monolithic two-stage differential input, differential output video amplifier. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. This device provides fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option

100000235 100000327 100000339

Pin Configuration



Triple 3-Input Positive-NAND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

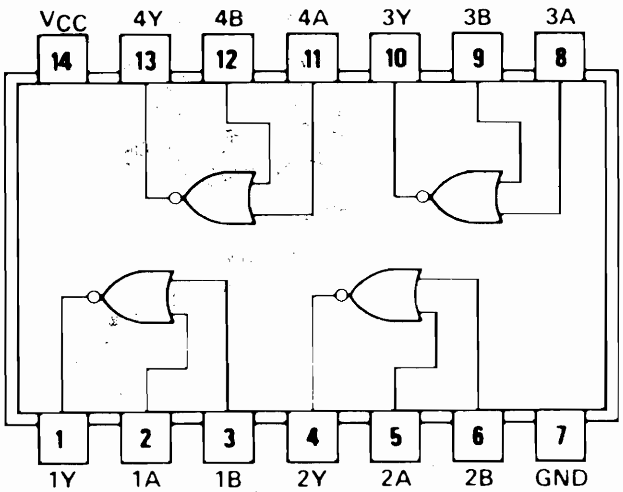
Positive logic: $Y = \overline{ABC}$

Note: The 100000235 is a Schottky device.

100000262 100000330
100000341 100000366

Quadruple 2-Input Positive-NOR Gate

Pin Configuration



Logic Diagram/Pin Designations

V_{CC} = Pin 14

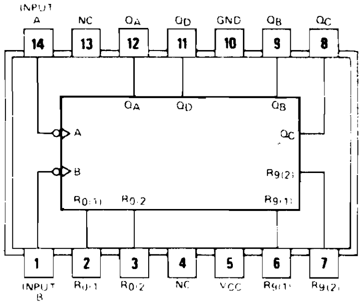
Gnd = Pin 7

Positive logic: $Y = \overline{A+B}$

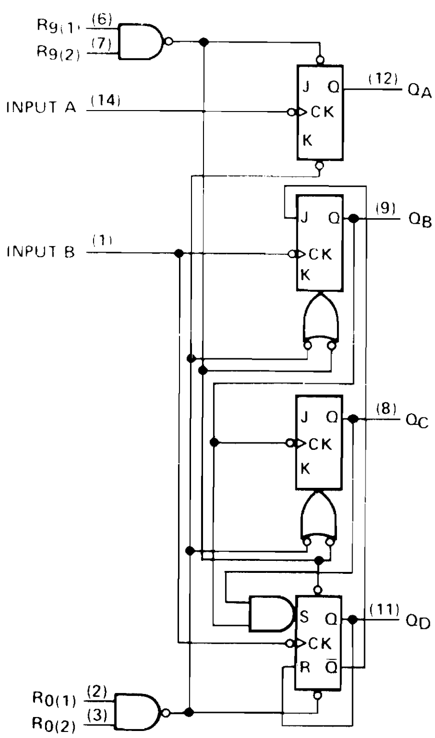
REV. 03

100000331 100000391 100000392

Pin Configuration
100000391



Functional Block Diagram
100000391



4-Bit Binary and Decade Counters

Pin Designations

V_{CC} = Pin 5
Gnd = Pin 10
NC = No internal connections

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 100000391, and divide-by-eight for the 100000331 and 100000392.

All of these counters have a gated zero reset and the 100000391 also has gated set-to-nine inputs for use in BCD nine's complement applications.

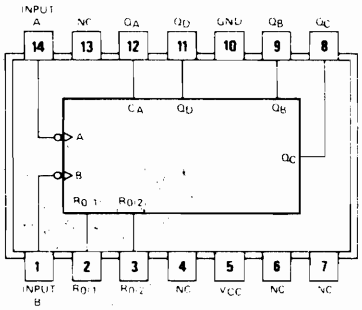
Notes:

1. The B input is connected to the Q_A output.
2. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.
3. A symmetrical divide-by-ten count can be obtained from the 100000391 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

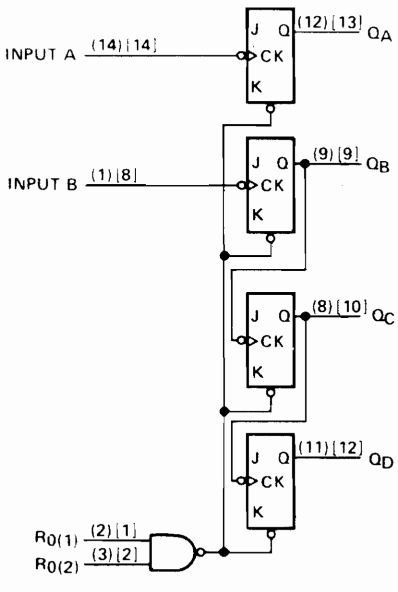
Continued....

100000331 100000391 100000392

Pin Configuration
100000331, 100000392



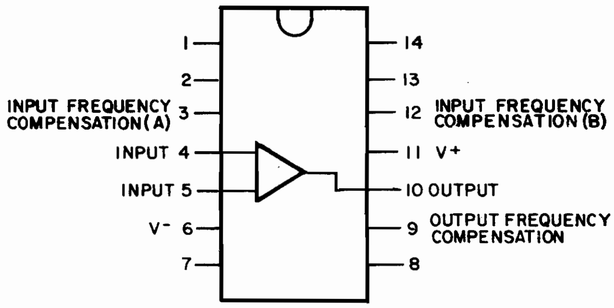
Functional Block Diagram
100000331, 100000392



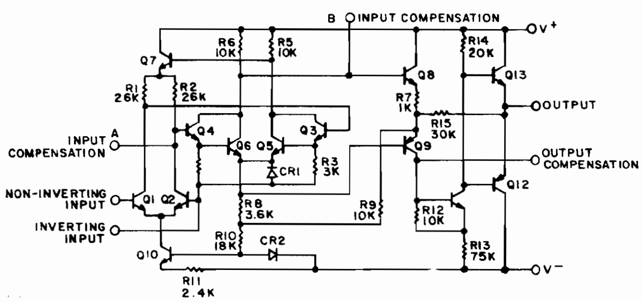
Continued....

100000333 100000344

Pin Configuration



Schematic Diagram



Operational Amplifier

Pin Designations

V+ = Pin 11

V- = Pin 6

The 100000333 is a monolithic operational amplifier. Operation is completely specified over the range of voltages commonly used for these devices. The design, in addition to providing high gain, minimizes both offset voltage and bias currents. The class B output stage gives a large output capability with minimum power drain.

External components are used to frequency compensate the amplifier. Compensation can be tailored to optimize high-frequency performance for any gain setting.

Note:

The 100000344 is the commercial-industrial version of the 100000333. It is identical to the 100000333 except that it is specified for operation from 0 °C to 70 °C.

100000317 100000334

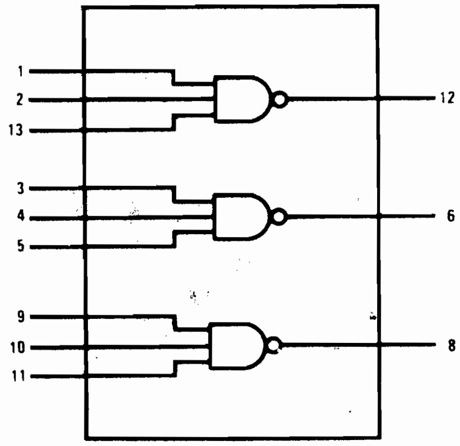
Triple Three Input NAND Gate

Pin Designations

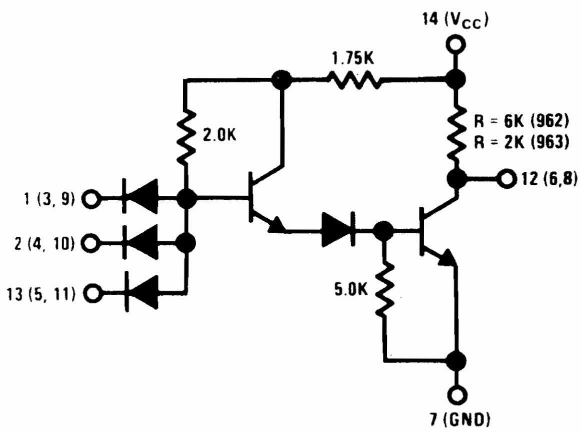
V_{CC} = Pin 14

Gnd = Pin 7

Connection/Logic Diagram



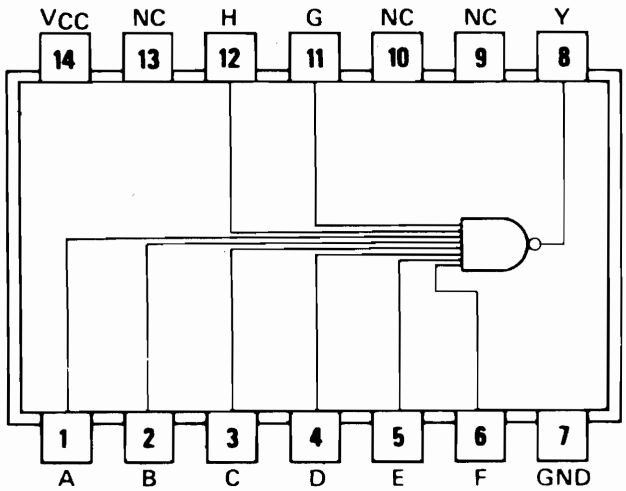
Schematic Diagram



REV. 03

100000195 100000337

Pin Configuration



8-Input Positive-NAND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

NC = No internal connection

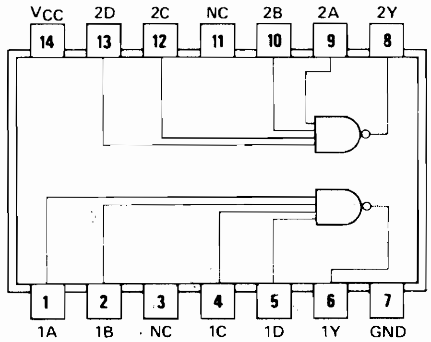
Positive logic: $Y = \overline{ABCDEFGH}$

REV. 03

100000338

Dual 4-Input Positive-Nand Buffers

Pin Configuration



Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

NC = No internal connections

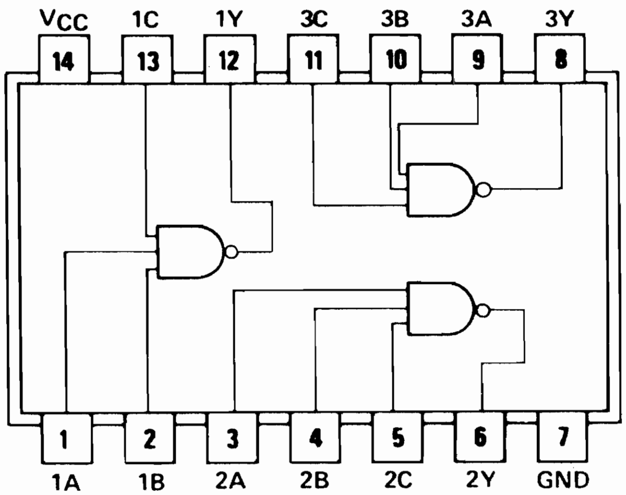
Positive logic $Y=\overline{ABCD}$

REV. 03

100000235 100000327 100000339

Triple 3-Input Positive-NAND Gate

Pin Configuration



Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

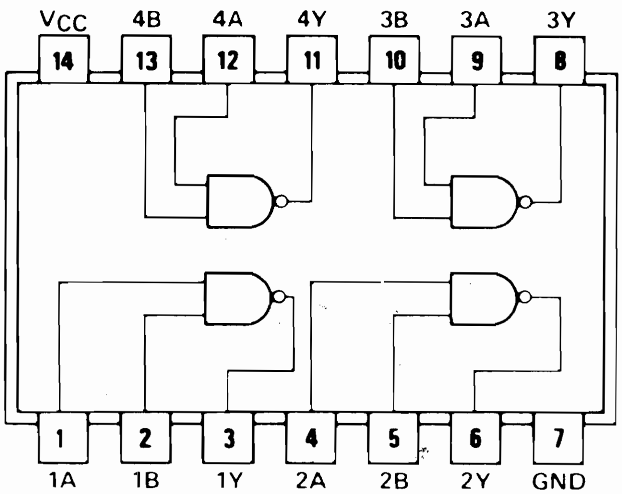
Positive logic: $Y = \overline{ABC}$

Note: The 100000235 is a Schottky device.

REV. 03

100000158 100000340 100000515

Pin Configuration



Quadruple 2-Input Positive-NAND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

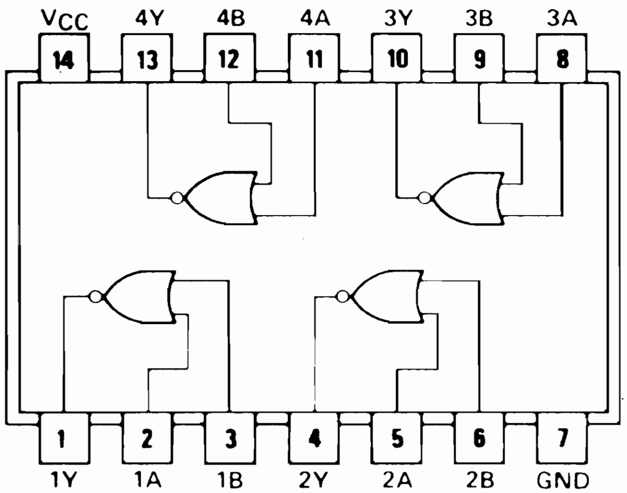
Positive logic: $Y = \overline{AB}$

Note: The 100000158 is a Schottky device.

REV. 03

100000262 100000330
100000341 100000366

Pin Configuration



Quadruple 2-Input Positive-NOR Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

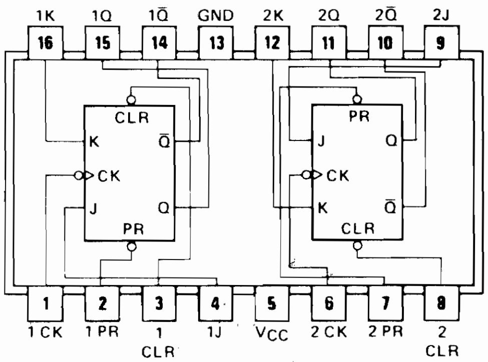
Positive logic: $Y = \overline{A+B}$

REV. 03

100000342

Dual J-K Flip-Flops With Preset and Clear

Pin Configuration



Pin Designations

V_{CC} = Pin 5

Gnd = Pin 13

Function Table

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

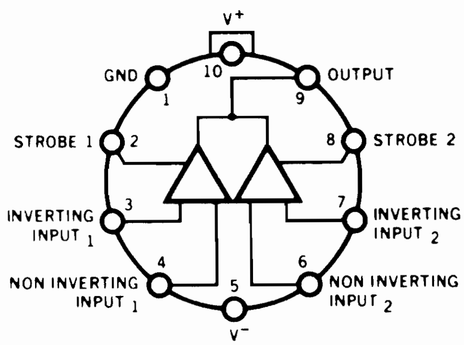
*This configuration is nonstable; that is it will not persist when preset and clean inputs return to their inactive (high) state.

REV. 03

100000060 100000343

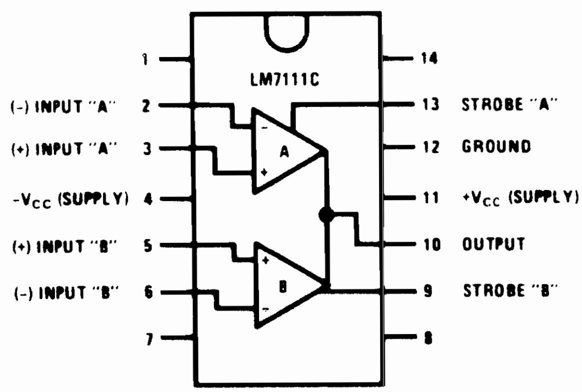
Dual Comparator

Pin Configuration



100000060

Dual-In-Line Package



100000343

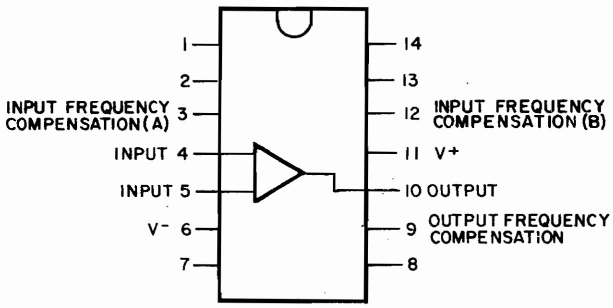
This device is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms.

When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided.

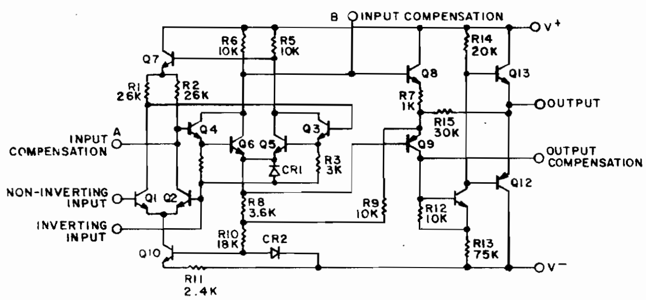
100000333 100000344

Operational Amplifier

Pin Configuration



Schematic Diagram



Pin Designations

V+ = Pin 11

V- = Pin 6

The 100000333 is a monolithic operational amplifier. Operation is completely specified over the range of voltages commonly used for these devices. The design, in addition to providing high gain, minimizes both offset voltage and bias currents. The class B output stage gives a large output capability with minimum power drain.

External components are used to frequency compensate the amplifier. Compensation can be tailored to optimize high-frequency performance for any gain setting.

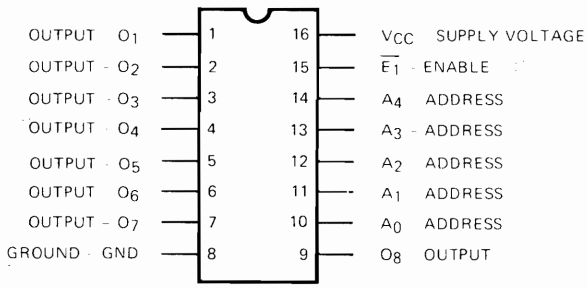
Note:

The 100000344 is the commercial-industrial version of the 100000333. It is identical to the 100000333 except that it is specified for operation from 0℃ to 70℃.

100000258 100000347 100000348 100000349 100000350 100000351 100000352 100000353 100000485 100000486

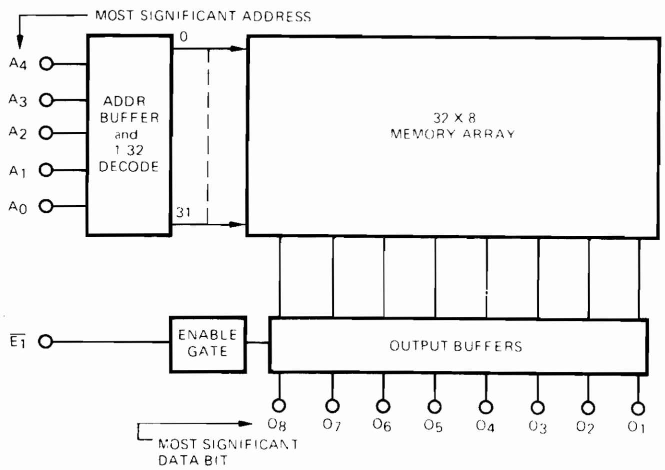
256 Bit Bipolar (32x8) Electrically Programmable Read Only Memory

Pin Configuration



Low = Enable

Block Diagram



This device is a field programmable, 256-bit, DTL and TTL compatible, bipolar read only memory.

The three-state output of this device provides a low impedance driver Q_2 for driving capacitance on the memory output; no pullup resistor is required. When the chip enable is low, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. In a system enviornment, up to 21 memory outputs of the read only memory can be connected to a common bus. All of the devices, except one, are placed in the high impedance state. The selected device is enabled and has the characteristics of a TTL totem pole output.

Memory Operation

The memory is addressed with inputs A_0 through A_4 which select one of 32 words. To enable the outputs for a readout, enable E_1 must be low. If the enable is high, the outputs are held off permitting wire "OR"ing of the three-state outputs of several packages. The use of the enable permits expansion to greater than 32 words.

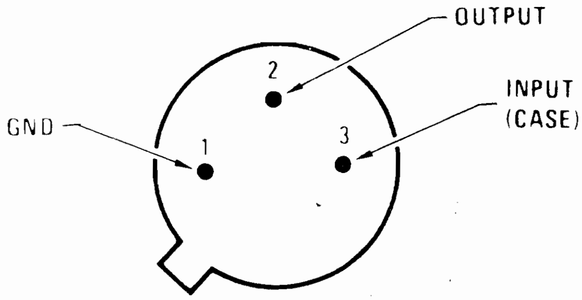
100000290 100000354 100000379

Three-Terminal Negative Regulator

The 100000290, 100000354, and the 100000379 are three-terminal negative regulators. The 100000290 and the 100000354 have fixed output voltages of -12V and the 100000379 has a fixed output voltage of -5V. These devices need only one external component--a compensation capacitor at the output.

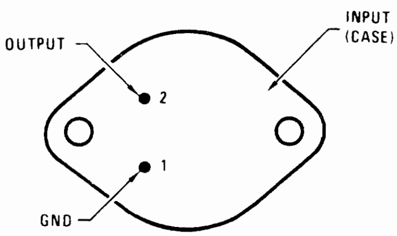
Pin Configuration

3-Lead Metal Box



BOTTOM VIEW

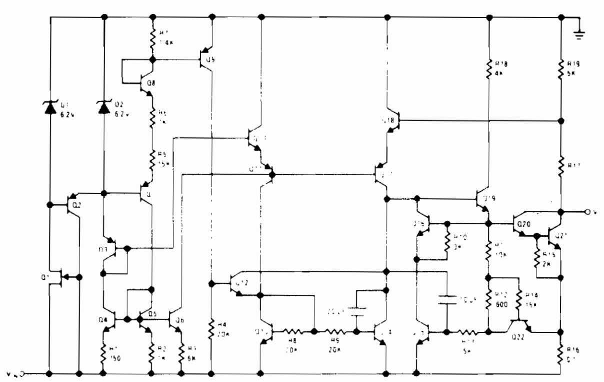
100000290



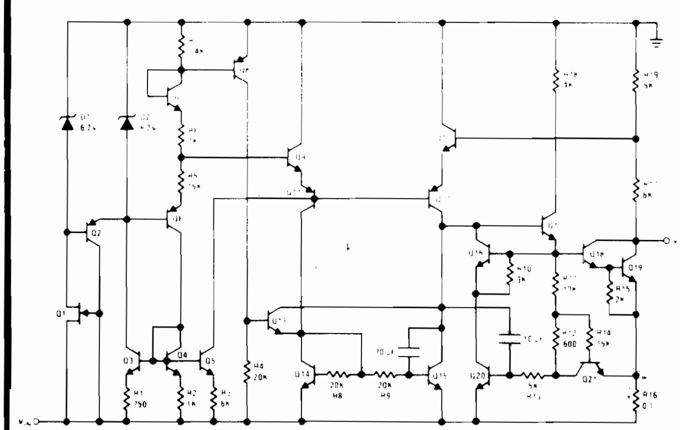
BOTTOM VIEW

100000354, 100000379

Schematic



100000290, 100000354

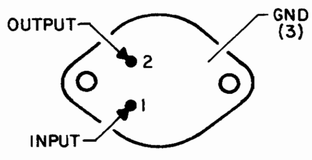


100000379

REV. 03

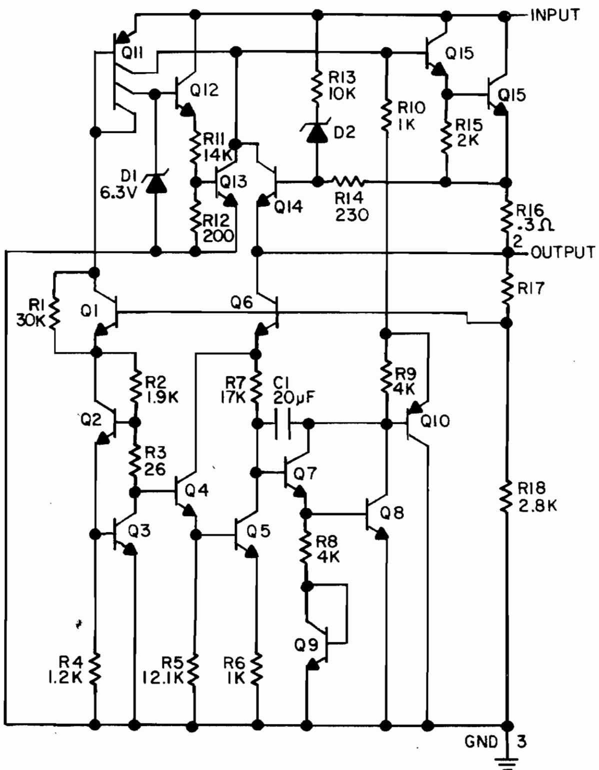
100000355

Pin Configuration



BOTTOM VIEW

Schematic



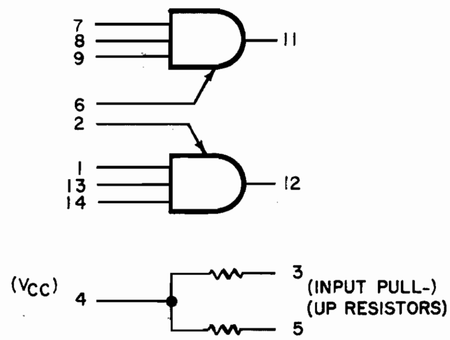
Three Terminal Positive Regulator

The 100000355 Positive Regulator provides over 1. 0 Amp of output current if adequate heat sinking is provided. Current limiting keeps the peak output current to a safe value. Safe area protection limits internal power dissipation. The thermal shutdown circuit prevents the IC from overheating when power dissipation exceeds the capacity of the heat sink.

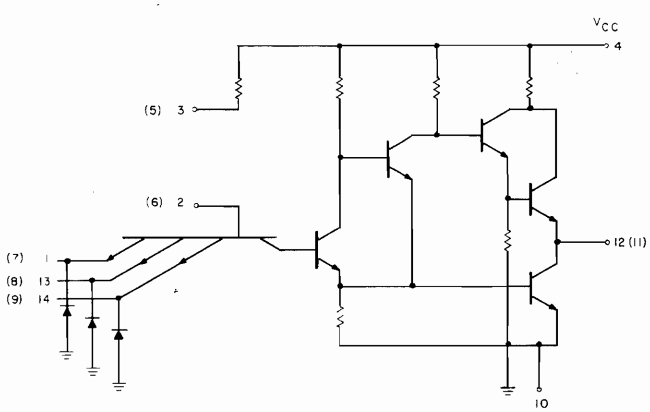
100000023 100000356 100000357

Dual Pulse Shaper-Delay AND Gate

Logic Diagram

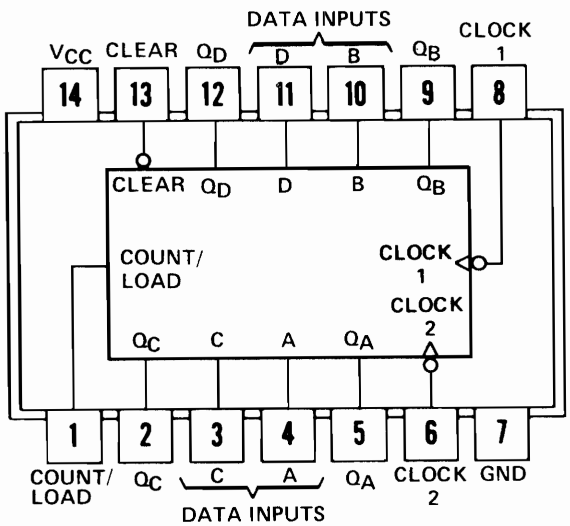


Schematic



100000358

Pin Configuration



35-MHz Presettable Decade

Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

The 100000358 is a high-speed monolithic counter consisting of four d-c coupled master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-eight counter. The outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the inputs independent of the state of the clocks.

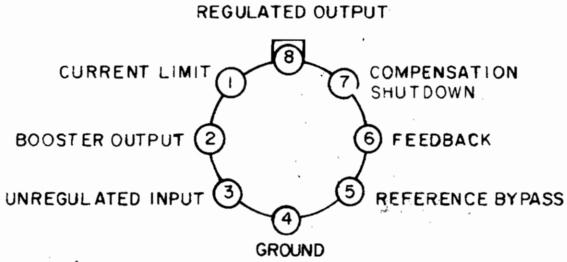
This counter may also be used as a 4-bit latch by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count load is high and the clock inputs are inactive.

The 100000358 will accept count frequencies of 0 to 35 megahertz at the clock-1 input and 0 to 17.5 megahertz at the clock-2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission-line effects. The circuits are compatible with most TTL and DTL logic families.

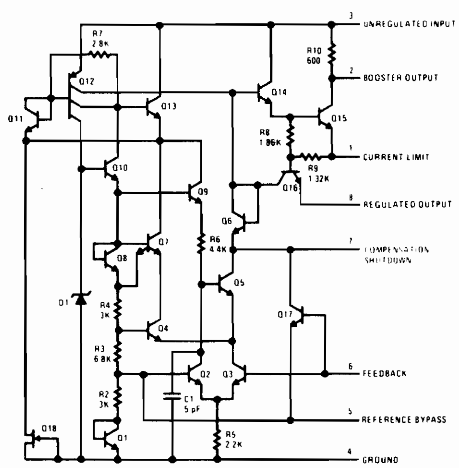
100000359 100000380

Pin Configuration
Metal Can



Note Pin 4 connected to case
TOP VIEW

Schematic



Positive Voltage Regulator

The 100000359 and the 100000380 are positive voltage regulators. The design of the biasing circuitry removes any minimum load current requirement and at the same time reduces standby current drain, permitting higher voltage operation.

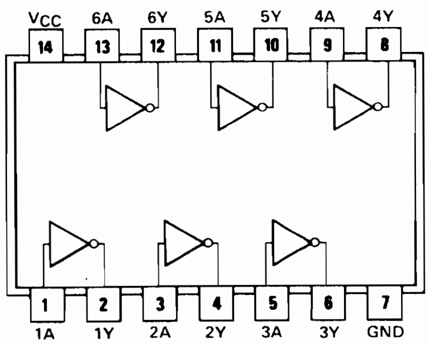
These regulators also feature fast response to both load and line transients, freedom from oscillations with varying resistive and reactive loads and the ability to start reliably on any load within rating.

Note:

The 100000359 is specified for operation from -25 °C to 85 °C. The 100000380 is specified for operation from 0 ° C to 70 °C and for output voltages to 30V.

100000360

Pin Configuration



Hex Inverter

Pin Designations

V_{CC} = Pin 14

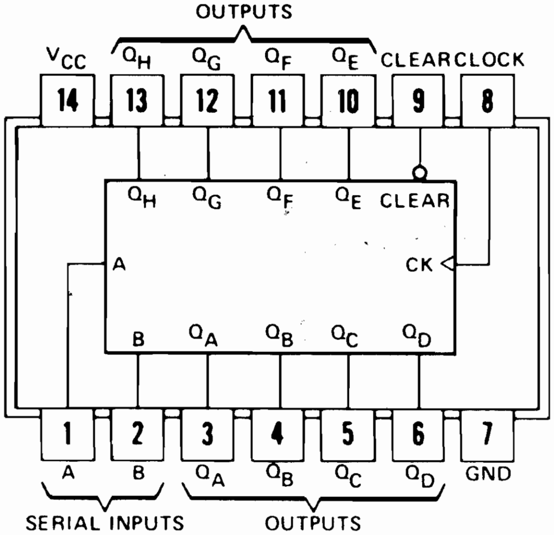
Gnd = Pin 7

Positive logic: $Y=\overline{A}$

100000362

8-Bit Parallel-Out Serial-Shift Register

Pin Configuration



Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B ...	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level.

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock, indicates a one-bit shift.

The 100000362 features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

REV. 03

100000309 100000363

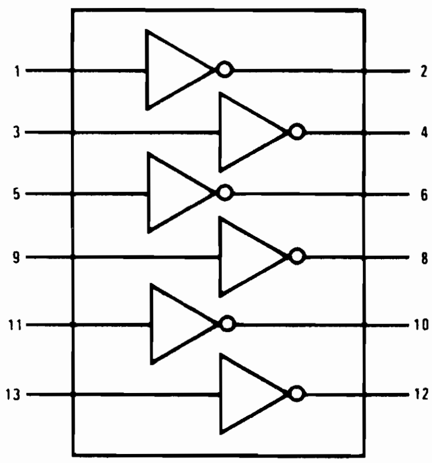
Hex Inverter

Pin Designations

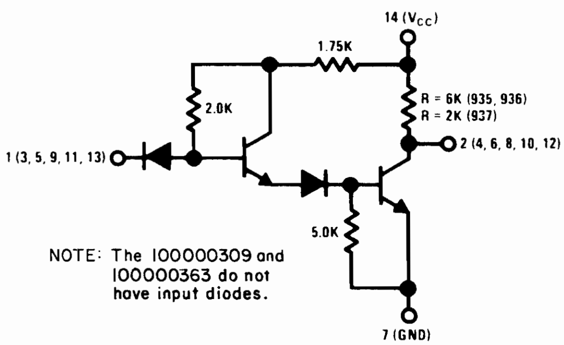
V_{CC} = Pin 14

Gnd = Pin 7

Connection/Logic Diagram



Schematic Diagram



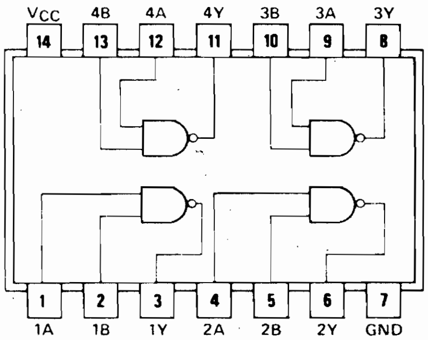
NOTE: The 100000309 and 100000363 do not have input diodes.

REV. 03

100000364

Quadruple 2-Input Positive-NAND Gate with Open-Collector Outputs

Pin Configuration



Pin Designations

V_{CC} = Pin 14

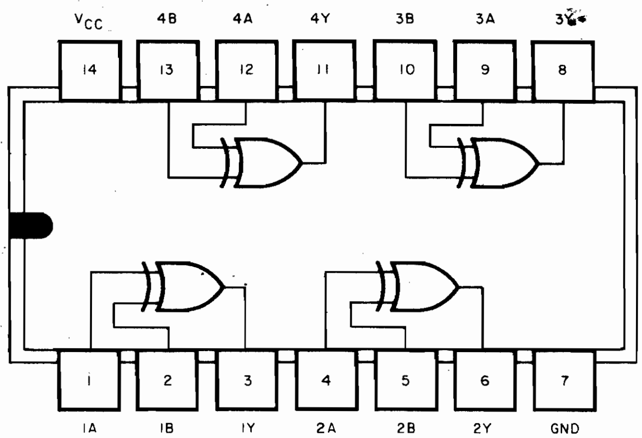
Gnd = Pin 7

Positive logic: $Y=\overline{AB}$

REV. 03

100000068 100000365

Pin Configuration



Quadruple 2-Input Exclusive-OR Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

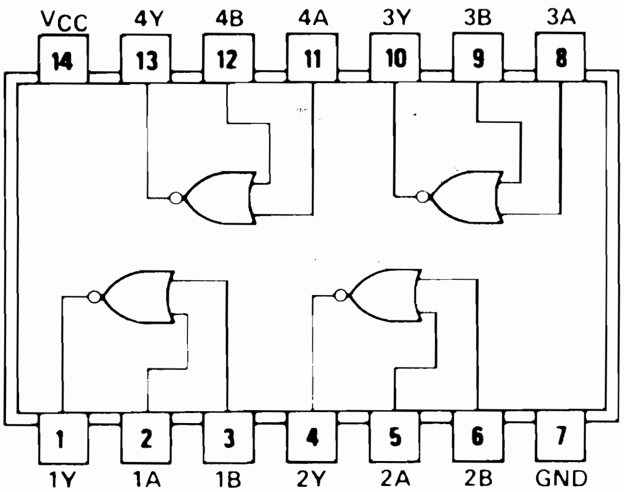
Positive logic: $Y = A \oplus B$

Note: The 100000365 is a Schottky device.

REV. 03

100000262 100000330
100000341 100000366

Pin Configuration



Quadruple 2-Input Positive-NOR Gate

Logic Diagram/Pin Designations

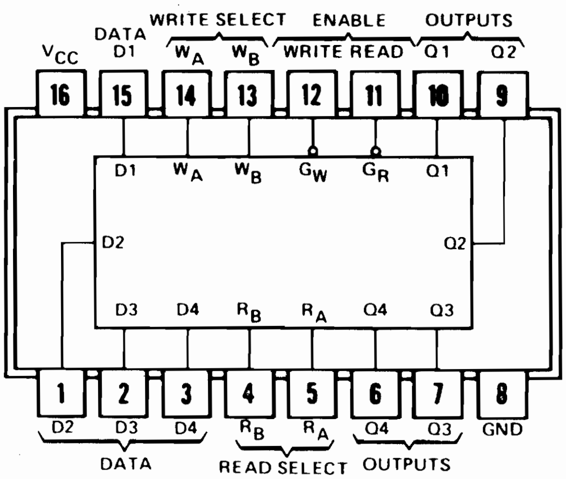
V_{CC} = Pin 14

Gnd = Pin 7

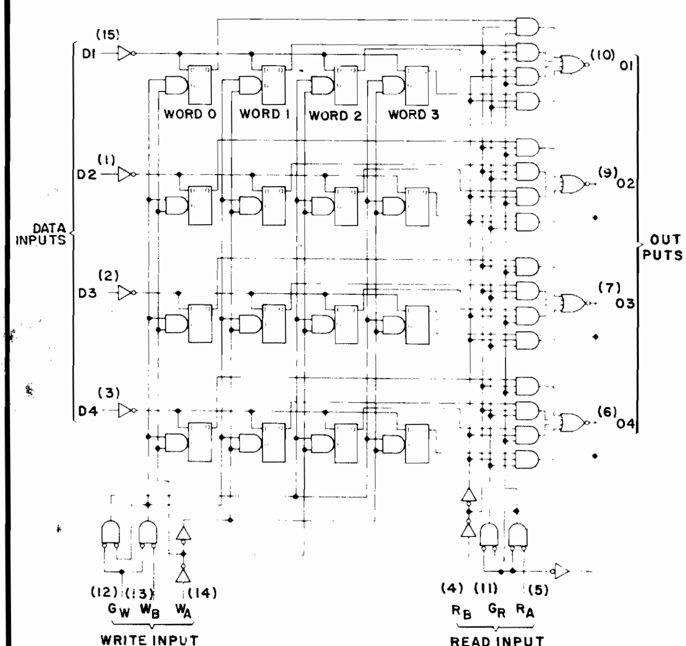
Positive logic: $Y = \overline{A+B}$

100000367

Pin Configration



Functional Block Diagram



4-By-4 Register Files with 3-State Outputs

Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

WRITE FUNCTION TABLE

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

NOTES:
A. H = high level,
L = low level,
X = irrelevant,
Z = high impedance (off)

B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

C. Q_0 = the level of Q before the indicated input conditions were established.

D. W0B1 = The first bit of word 0, etc.

Continued....

REV. 03

100000367

Continued

The 100000367 16-bit TTL register file incorporates the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and seperate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form; that is, is a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

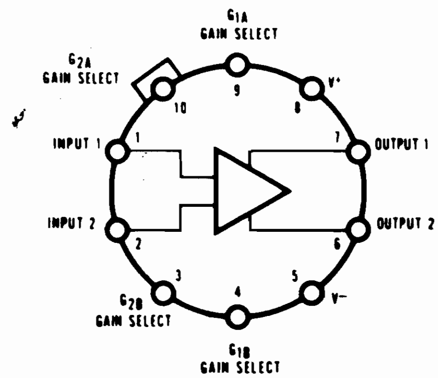
All inputs except read enable and write enable are buffered to lower the drive requirements. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

The 100000367 is characterized for operation from 0°C to 70°C.

100000062 100000314
100000326 100000372

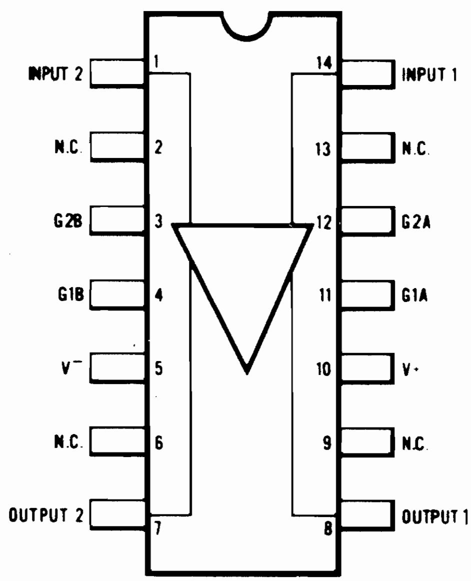
Pin Configuration

Top View



100000062, 100000326

TO-116 DUAL IN-LINE



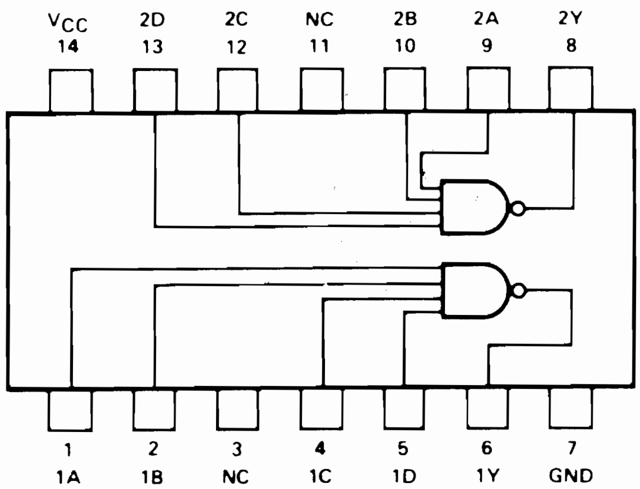
100000314, 100000372

Differential Video Amplifier

This device is a monolithic two-stage differential input, differential output video amplifier. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. This device provides fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option.

100000249 100000374

Pin Configuration



Positive-NAND Gate

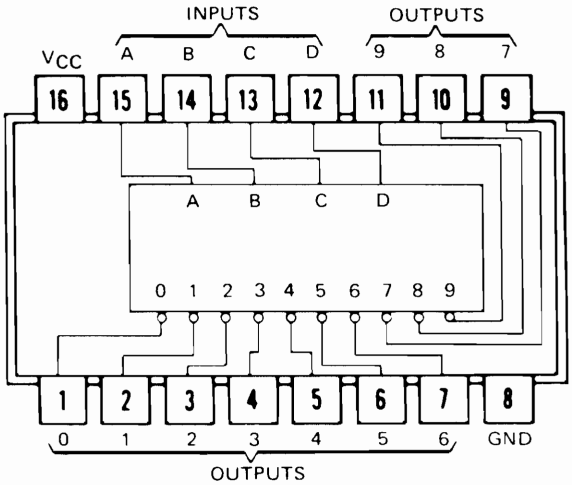
Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

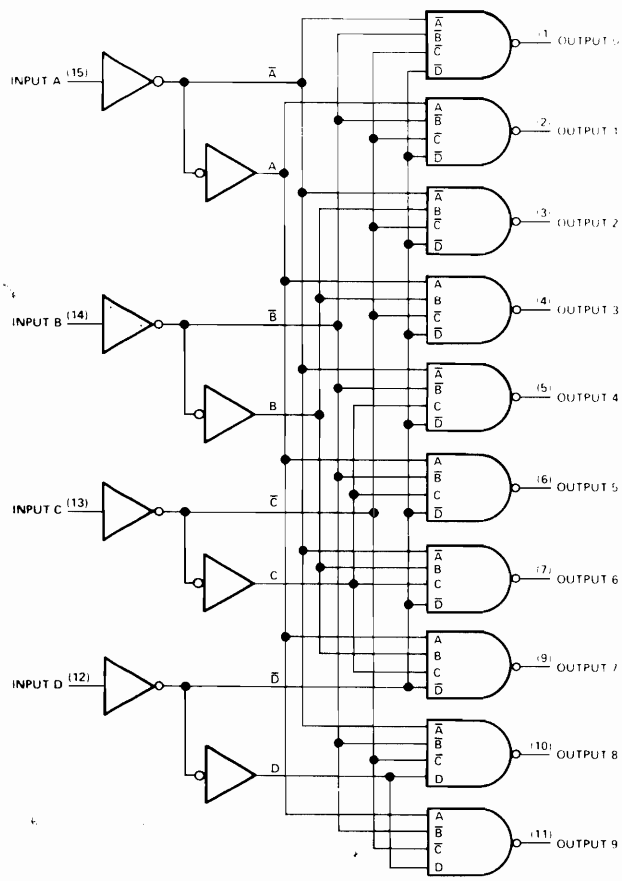
Note: The 100000249 is a Schottky device.

100000375

Pin Configuration



Functional Block Diagram



BCD To Decimal Decoder

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Input/Output Truth Table

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

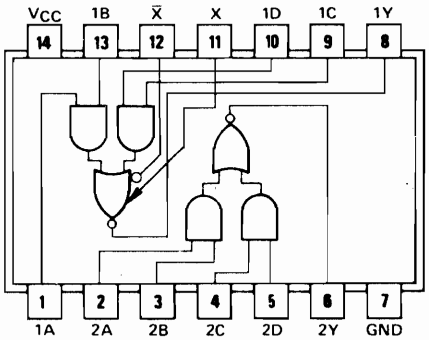
H = high level, L = low level

The 100000375 is a monolithic decimal decoder consisting of eight inverters and ten four-input Nand gates. The inverters are connected in pairs to make BCD input data available for decoding by the Nand gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions. This device features familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt.

100000376

Dual 2-Wide 2-Input AND-OR-INVERT Gates (One Gate Expandable)

Pin Configuration



Pin Designations

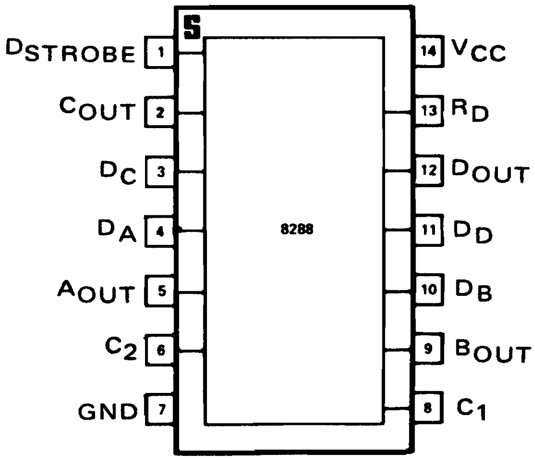
V_{CC} = Pin 14

Gnd = Pin 7

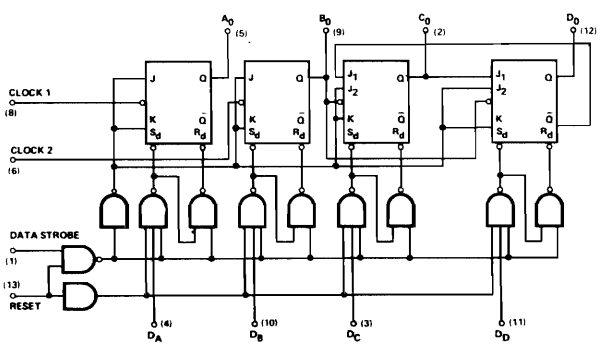
Positive logic: $\overline{Y=AB+CD+X}$

100000377

Pin Configuration



Logic And Connection Diagram



V_{CC} = (14) A,F PACKAGES
GND = (7)
( ) = Denotes Pin Numbers for 14 Pin Dual-in-Line Package

Divide-By-Twelve Counter/Storage Element

Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

	OUTPUT			
Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

*Connected for Divide-by-Twelve operation (output A connected to CP2)

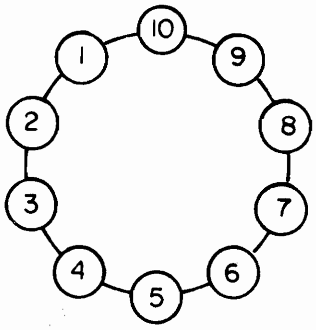
The 100000377 Divide-by-Twelve Counter is a four-bit subsystem consisting of divide by two and divide by six counters in a 14 pin package. For Divide-by-Twelve operation, output A is connected externally to the clock 2 input.

The 100000377 has strobed paralleled data entry capability so that the counter may be preset to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at a "0" level. For additional flexibility, this device is provided with a common reset. A "0" on the reset line produces "0" at all four outputs.

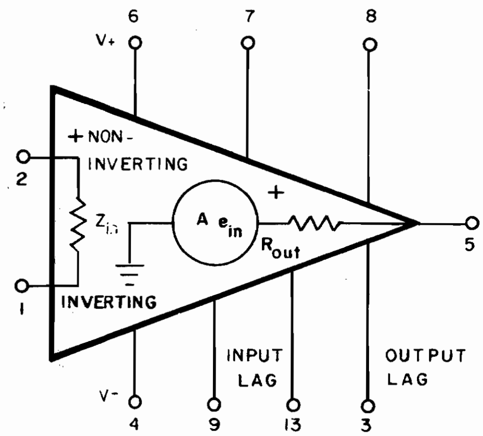
The counting operation is performed on the falling (negative going) edge of the input clock pulse, however, there is no restriction on transition time since the individual binaries are level sensitive. The data strobe and reset funcitons are asynchronous with respect to the clock.

100000378

Pin Configuration



Equivalent Circuit



Monolithic Operational Amplifier

Pin Designations

1. A
2. B
3. C Output Lag
4. D V-
5. E
6. F V+
7. G
8. H
9. J Input Lag
10. K

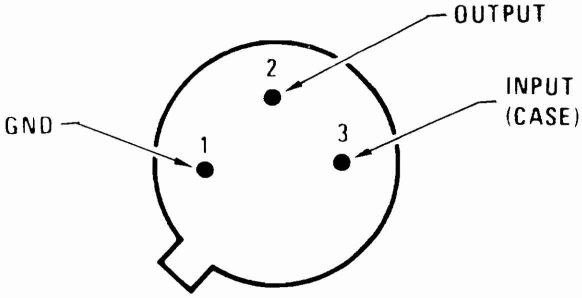
The 100000378 is a monolithic operational amplifier designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

100000290 100000354 100000379

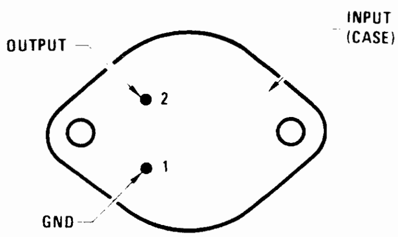
Three-Terminal Negative Regulator

The 100000290, 100000354, and the 100000379 are three-terminal negative regulators. The 100000290 and the 100000354 have fixed output voltages of -12V and the 100000379 has a fixed output voltage of -5V. These devices need only one external component--a compensation capacitor at the output.

Pin Configuration
3-Lead Metal Box

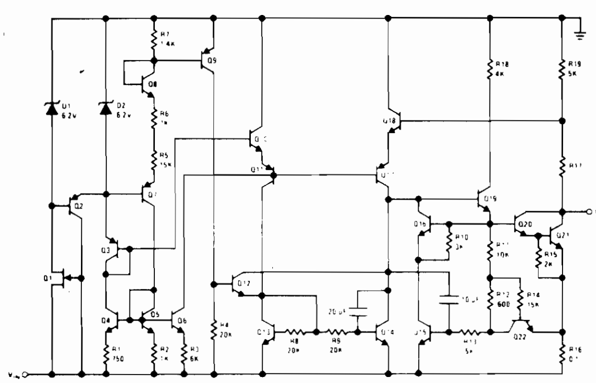


BOTTOM VIEW
100000290

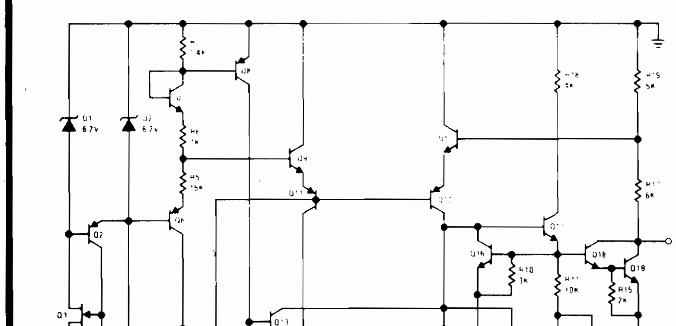


BOTTOM VIEW
100000354, 100000379

Schematic



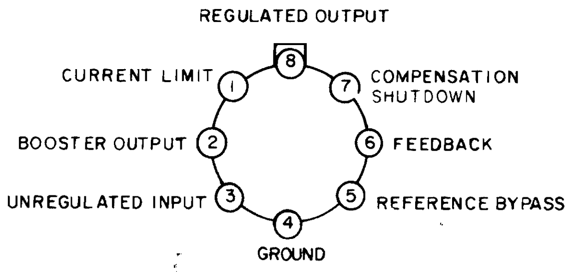
100000290, 100000354



100000379

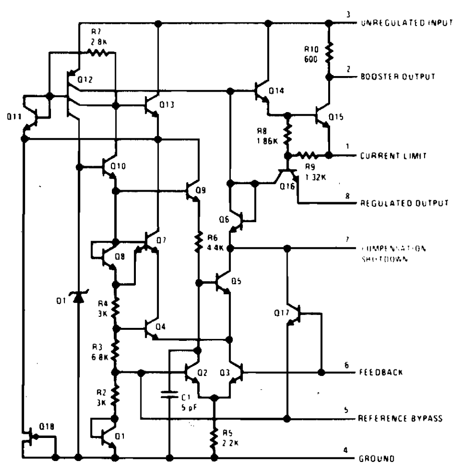
100000359 100000380

Pin Configuration
Metal Can



Note Pin 4 connected to case
TOP VIEW

Schematic



Positive Voltage Regulator

The 100000359 and the 100000380 are positive voltage regulators. The design of the biasing circuitry removes any minimum load current requirement and at the same time reduces standby current drain, permitting higher voltage operation.

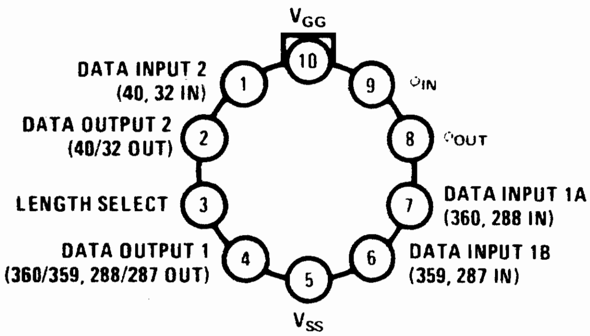
These regulators also feature fast response to both load and line transients, freedom from oscillations with varying resistive and reactive loads and the ability to start reliably on any load within rating.

Note:

The 100000359 is specified for operation from -25°C to 85°C. The 100000380 is specified for operation from 0°C to 70°C and for output voltages to 30V.

100000381

Pin Configuration
Metal Can Package



TOP VIEW

Dynamic Shift Register

Pin Designations

V_{SS} = Pin 5

V_{GG} = Pin 10

The 100000381 360/359, 228/287, 40/32 bit dynamic shift register is a monolithic MOS integrated circuit utilizing p-channel enhancement mode low threshold technology to achieve bipolar compatibility. The register lengths are lengthened or shortened by hard wiring the length select line to V_{GG} or V_{SS}. This device features DTL/TTL compatibility.

100000109 100000125 | 100000111 100000382

Buffer Registers

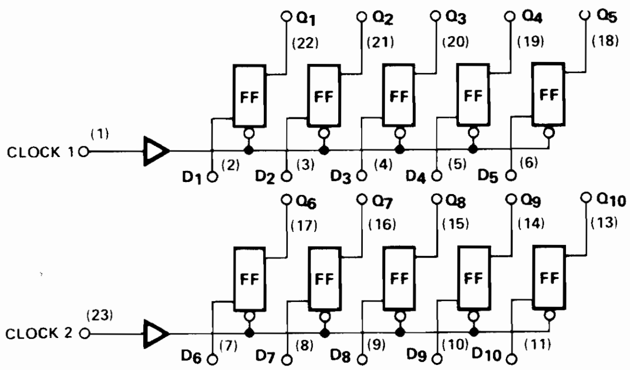
Logic Diagram/Pin Designations

V_{CC} = Pin 24

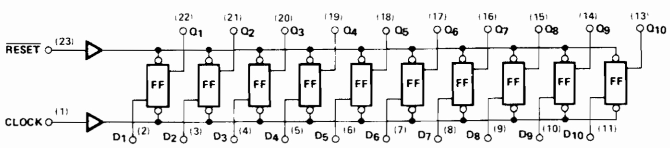
Gnd = Pin 12

Logic Diagrams

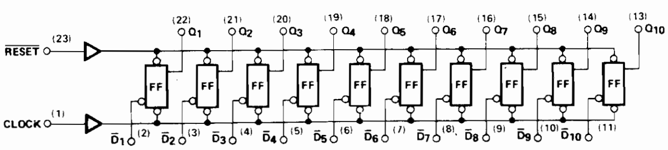
100000111, 100000382



100000109



100000125



Truth Tables

Dual 5-Bit Buffer Registers Nos. 100000111 and 100000382

D_n	Q_{n+1}
1	1
0	0

10-Bit Buffer Register No. 100000109

D_n	$\overline{RESET}$	Q_{n+1}
1	1	1
0	1	0

10-Bit Buffer Register-Inverted Inputs No. 100000125

D_n	$\overline{RESET}$	Q_{n+1}
0	1	1
1	1	0

Notes:

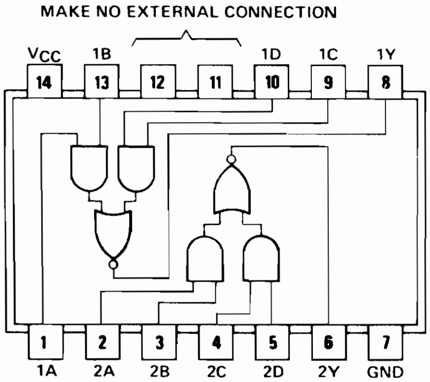
$\overline{RESET}$ = 0 ⇒ Q = 0 (overrides clock).
n is time prior to clock.
n+1 is time following clock.

These buffer registers are arrays of ten clocked "D" flip-flops. The flip-flops are arranged as a dual 5 array (100000111 & 100000382) and single 10 arrays with reset (100000109 and 100000125).

The 100000111, 100000382 and 100000109 have true "D" inputs. The logic state presented at these "D" inputs will appear at the Q outputs after a negative transition of the clock. The 100000125 has complementing "D" inputs ("$\overline{D}$"). The logic state presented at these "$\overline{D}$" inputs will invert and appear at the Q outputs after a negative-going transition of the clock. The complementing input ("$\overline{D}$") permits the use of standard AND-OR-INVERT gates to achieve the AND-OR function without additional gate delays.

100000383 100000504

Pin Configuration



Dual 2-Wide 2-Input AND-OR-INVERT Gates

Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

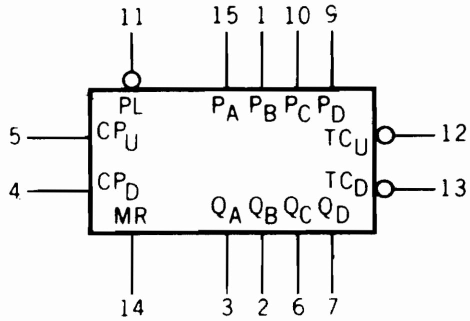
Positive logic: $Y=\overline{AB+CD}$

Note: 100000504 is a Schottky device.

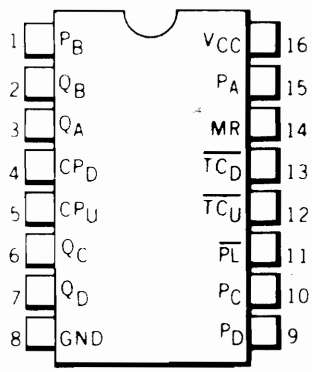
100000252 100000128 100000384

Up/Down Decade and Binary Counters

Logic Symbol

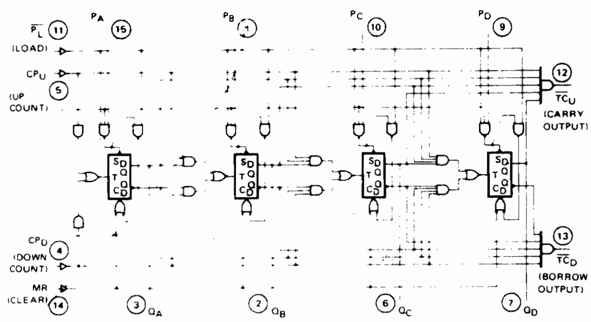


Pin Configuration

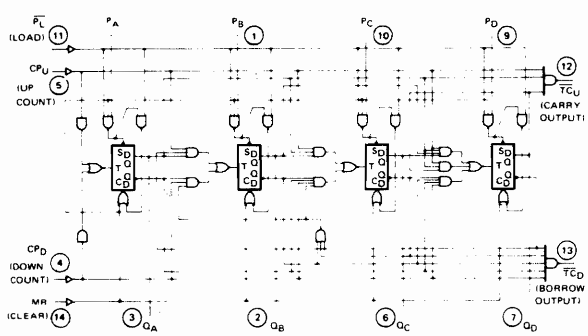


Logic Diagrams

100000128



100000252, 100000384



○ = PIN NUMBER

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Mode Selection
(Both Counters)

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

Notes:

H = High voltage level
L = Low voltage level
X = Don't care condition
CP = Clock pulse.

The 100000252 & 100000384 are synchronous Up/Down BCD Decade Counters and the 100000128 is a synchronous Up/Down 4-Bit Binary Counter. All these counters have separate up/down clocks, parallel load facility, terminal count outputs for multidecade operation and an asynchronous overriding master reset.

These counters can be reset, preset and count up or down. The operating modes are tabulated in the Mode Selection table. The operating modes of both devices are identical; the only difference between the devices is the count sequences.

Counting is synchronous, with the outputs changing state after the Low to High transition of either the Count-Up Clock (CP_U) or Count-Down Clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is High. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are Low simultaneously.) All counters will respond to a clock pulse on either input by changing to the next appropriate state of the count sequence. The state diagram for the 100000252 & 100000384 show the regular sequence and in addition shows the sequence of states if a code greater than nine is present in the counter.

Continued....

Logic Equations for Terminal Count

100000252 , 100000384

$$TC_U = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot \overline{CP_U}$$

$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

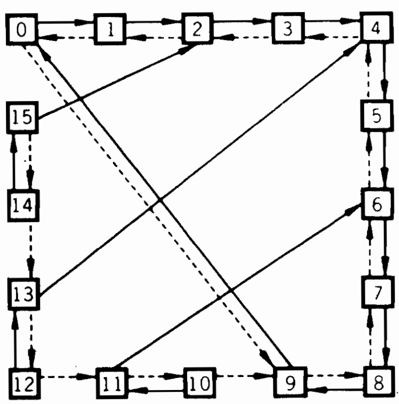
100000128

$$TC_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP_U}$$

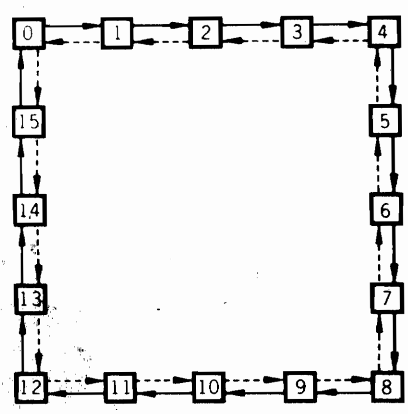
$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

State Diagrams

100000252, 100000384



100000128



COUNT UP ———

COUNT DOWN -------

All counters have a parallel load (asynchronous) facility which permits the device to be preset. Whenever the parallel load ($\overline{PL}$) input is Low, and Master Reset is Low, the information present on the Parallel Data inputs (P_A, P_B, P_C, P_D) will be loaded into the counters and appear on the outputs independent of the conditions of the clock inputs. When the Parallel Load Input goes High, this information is stored in the counters and when the counters are clocked they change to the next appropriate state in the count sequence. The Parallel Data inputs are inhibited when the Parallel Load is High and have no effect on the counters.

The Terminal Count-Up ($\overline{TC_U}$) and Terminal Count-Down ($\overline{TC_D}$) outputs (carry and borrow, respectively) allow multidecade counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and terminal count-down clock input of the following counter.

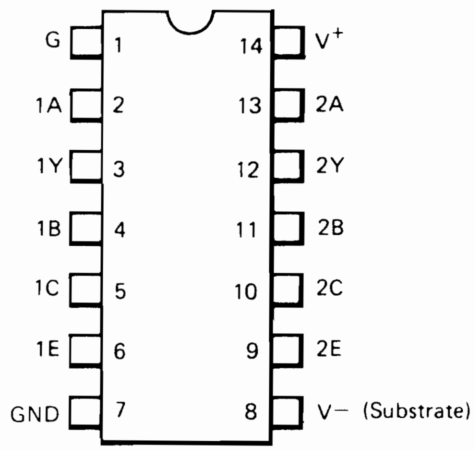
The terminal count-up outputs are Low when their count-up clock inputs are Low and the counters are in state nine (100000252 & 100000384) and state fifteen (100000128). Similarly, the terminal count-down outputs are Low when their count-down clock inputs are Low and both counters are in state zero. Thus, when the 100000252 & 100000384 counters are in state nine and the 100000128 counter is in state fifteen and all are counting up, or all counters are in state zero and counting down, a clock pulse will change the counter's state on the rising edge and simultaneously clock the following counter through the appropriate active Low terminal count output. There are two gate delays per state when these counters are cascaded.

The asynchronous Master Reset input (MR), when High, overrides all input and clears the counters. Master reset overrides parallel load so that when both are activated the counters will be reset. (Obviously, both parallel load and master reset must not be deactivated simultaneously for predictable operation.)

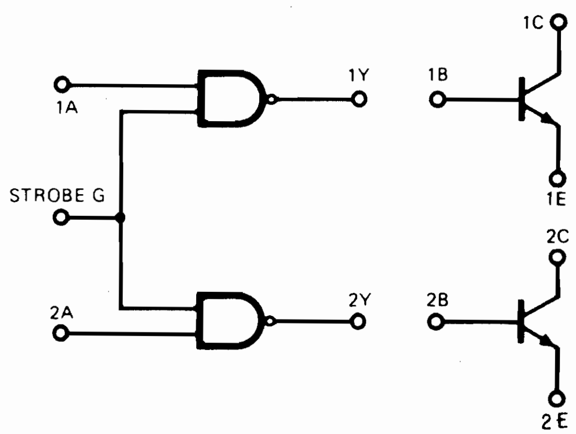
100000231 | 100000385

Dual Peripheral Driver

Pin Configuration



Functional Block Diagram



Pin Designations

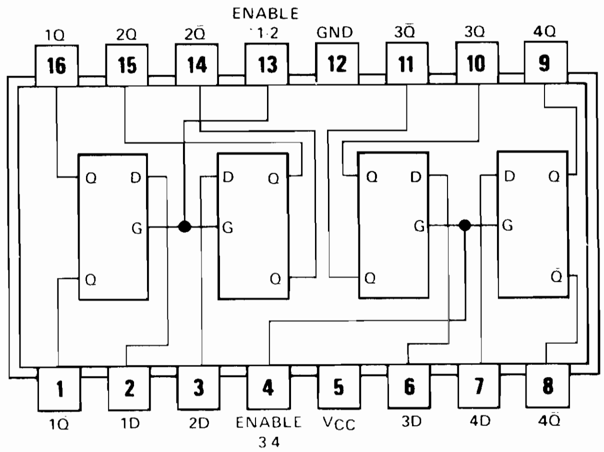
V+ = Pin 14

V- = Pin 8

Gnd = Pin 7

100000050 | 100000387

Pin Configuration



4-Bit Bistable Latches

Logic Diagram/Pin Designations

V_{CC} = Pin 5

Gnd = Pin 12

Function Table
(Each Latch)

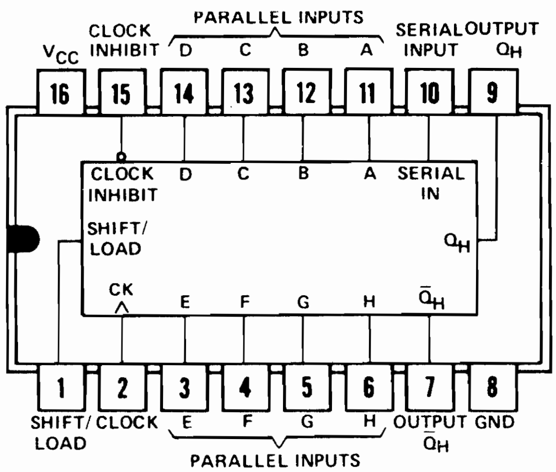
Inputs D	Inputs G	Ouputs Q	Ouputs $\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level; L = low level; X = irrelevant.
Q_0 = the level of Q before the high-to-low transition of G.

These latches are suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

100000389

Pin Configuration



Parallel-Load 8-Bit Shift Register

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

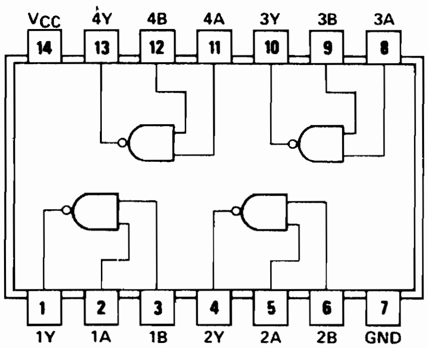
FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT Q_H
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	
L	X	X	X	a . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

REV. 03

100000390

Pin Configuration



Quadruple 2-Input Positive-NAND Gates With Open-Collector Outputs

Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

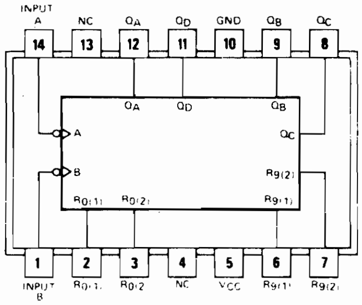
Positive logic: $Y=\overline{AB}$

REV. 03

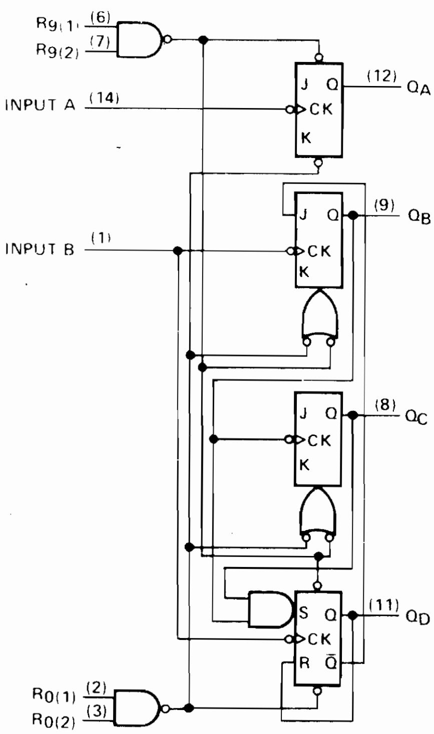
100000331 100000391 100000392

4-Bit Binary and Decade Counters

Pin Configuration
100000331, 100000392



Functional Block Diagram
100000391



Pin Designations

V_{CC} = Pin 5

Gnd = Pin 10

NC = No internal connections

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 100000391, and divide-by-eight for the 100000331 and 100000392.

All of these counters have a gated zero reset and the 100000391 also has gated set-to-nine inputs for use in BCD nine's complement applications.

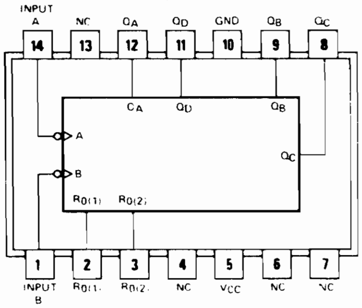
Notes:

1. The B input is connected to the Q_A output.
2. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.
3. A symmetrical divide-by-ten count can be obtained from the 100000391 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

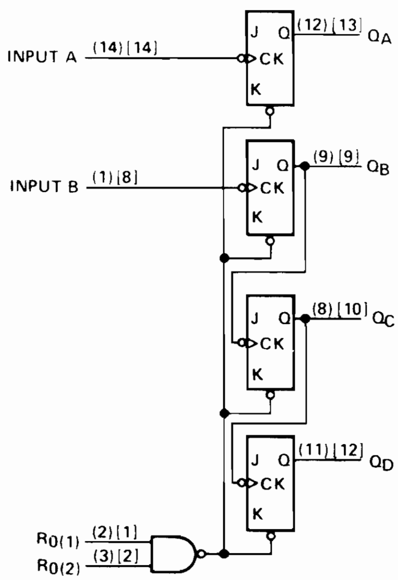
Continued....

100000331 100000391 100000392

Pin Configuration
100000331, 100000392



Functional Block Diagram
100000391

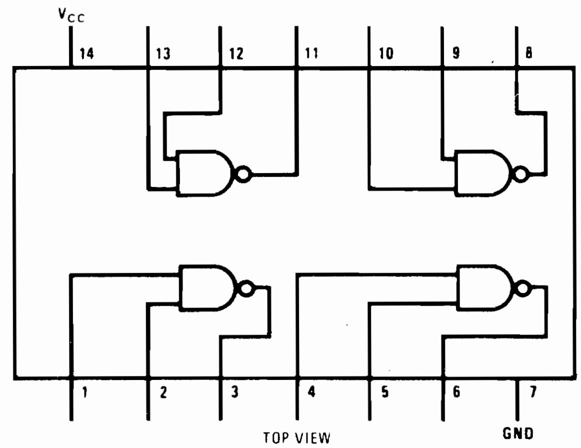


Continued....

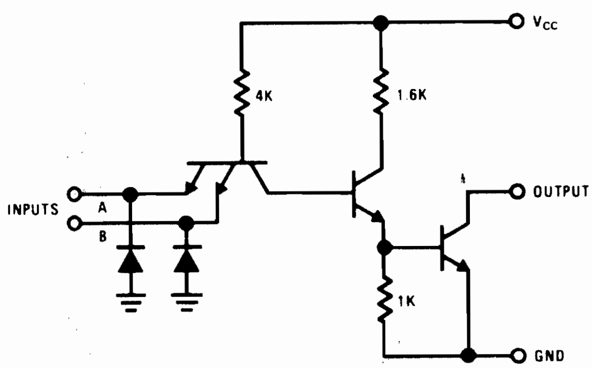
100000393

Quadruple 2-Input TTL-MOS Interface Gate

Pin Configuration



Schematic and Connection Diagram



Pin Designations

V_{CC} = Pin 14

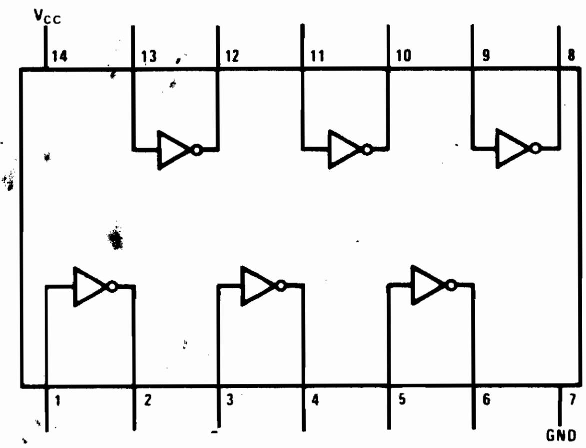
Gnd = Pin 7

REV. 03

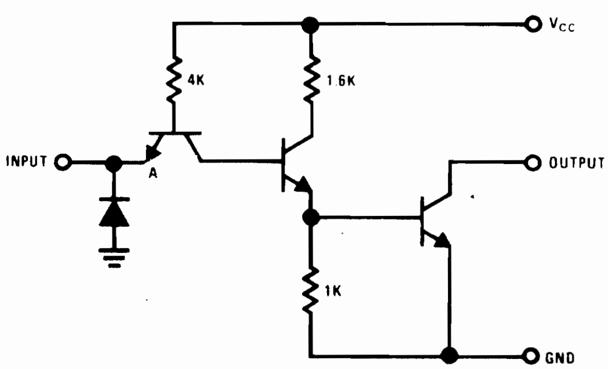
100000394

TTL-MOS Hex Inverter

Pin Configuration



Schematic



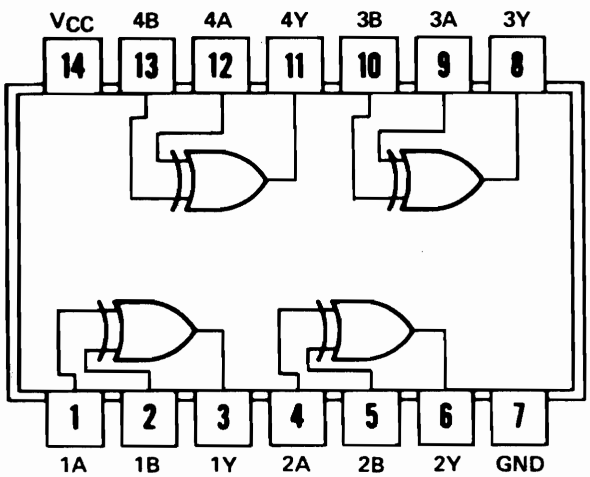
Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

100000399

Pin Configuration



Quadruple 2-Input Exclusive-or Gate with Open-Collector Output

Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

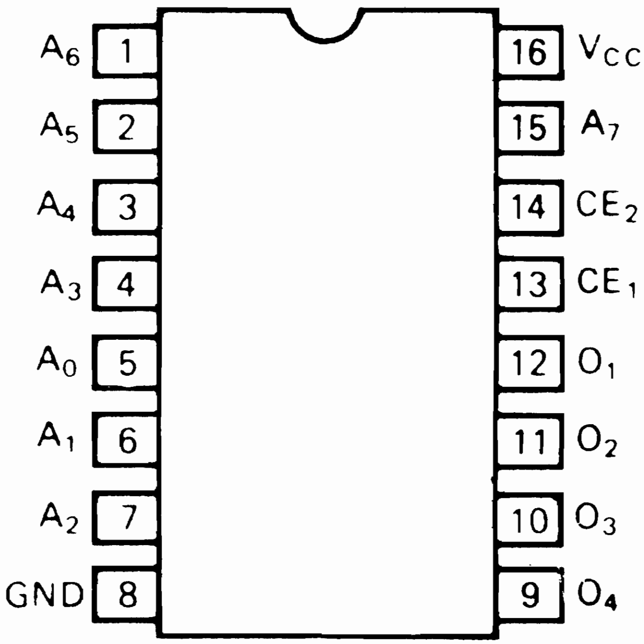
Positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE		
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

REV. 03

100000256
100000401 THRU 100000415
100000421 THRU 100000435
100000437 100000438
100000491 THRU 100000498

Pin Configuration



1024-Bit Programmable Bipolar Read Only Memory

Pin Designations

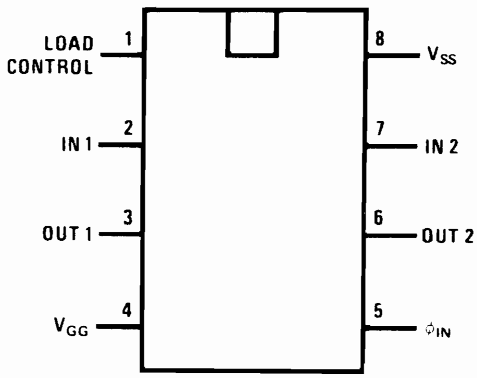
V_{CC} = Pin 16
Gnd = Pin 8

This integrated circuit is a high-speed, electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

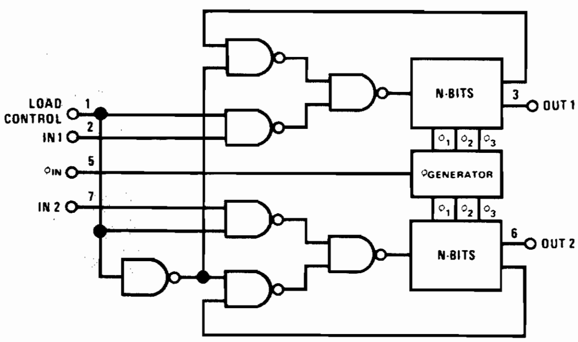
100000436

Pin Configuration



TOP VIEW

Logic and Connection Diagram



Dual 144-bit mask Programmable Static Shift Register

Pin Designations

V_{GG} = Pin 4

V_{SS} = Pin 8

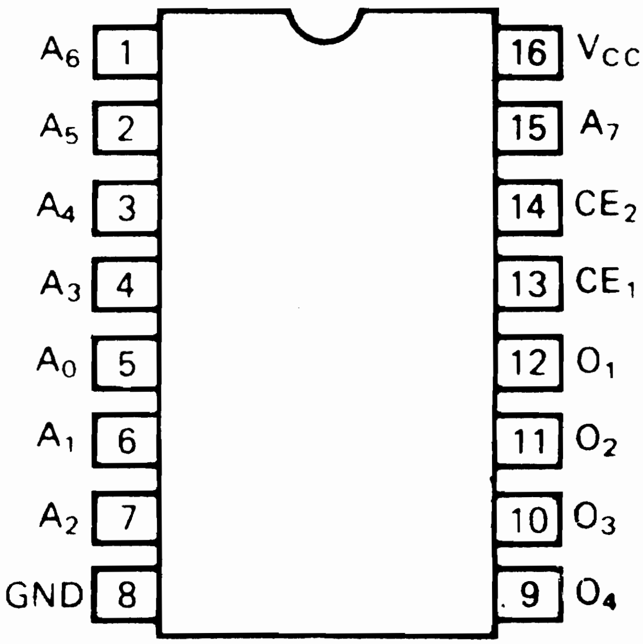
Truth Table

LOAD CONTROL	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

The 100000436 is a monolithic dual 144-bit static shift register/accumulator utilizing a silicon gate low threshold P-channel enhancement mode technology to achieve complete bipolar compatibility.

100000256
100000401 THRU 100000415
100000421 THRU 100000435
100000437 100000438
100000491 THRU 100000498

Pin Configuration



1024-Bit Programmable Bipolar Read Only Memory

Pin Designations

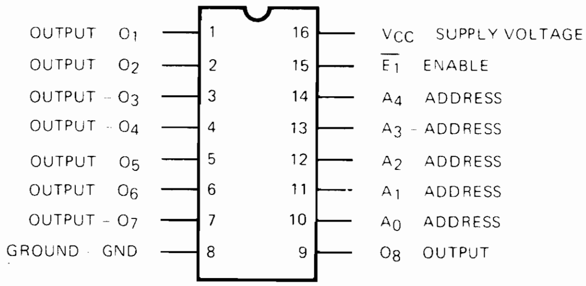
V_{CC} = Pin 16
Gnd = Pin 8

This integrated circuit is a high-speed, electrically programmable, full decoded TTL bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, two chip enable inputs and uncommitted collector outputs are provided.

The same address inputs are used for both programming and reading.

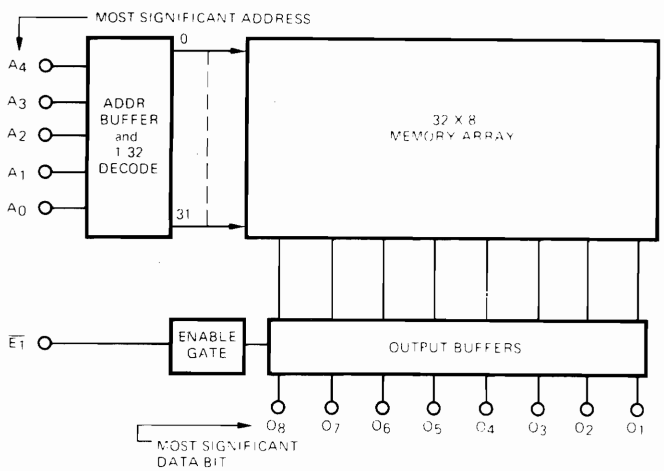
100000258 100000347 100000348 100000349 100000350 100000351 100000352 100000353 100000485 100000486

Pin Configuration



Low = Enable

Block Diagram



256 Bit Bipolar (32x8) Electrically Programmable Read Only Memory

This device is a field programmable, 256-bit, DTL and TTL compatible, bipolar read only memory.

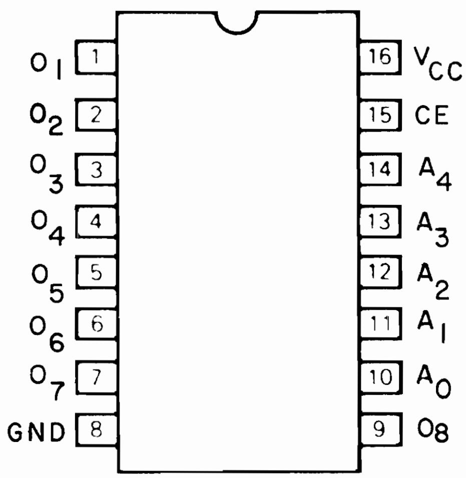
The three-state output of this device provides a low impedance driver Q_2 for driving capacitance on the memory output; no pullup resistor is required. When the chip enable is low, D_1 and D_2 are off and either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is high, D_1 and D_2 are on and Q_1 and Q_2 are off, permitting wire ORing of memory outputs. In a system enviornment, up to 21 memory outputs of the read only memory can be connected to a common bus. All of the devices, except one, are placed in the high impedance state. The selected device is enabled and has the characteristics of a TTL totem pole output.

Memory Operation

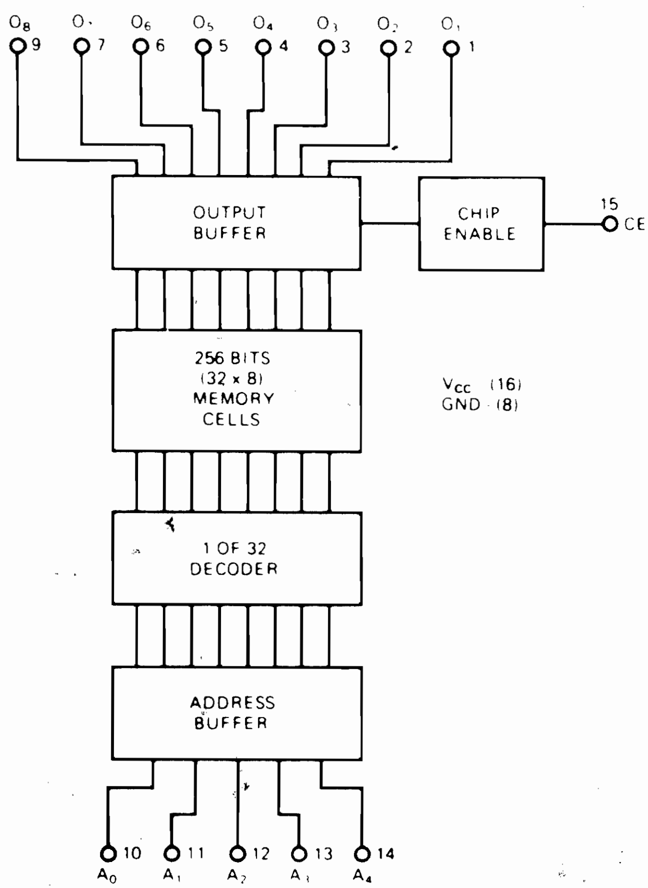
The memory is addressed with inputs A_0 through A_4 which select one of 32 words. To enable the outputs for a readout, enable E_1 must be low. If the enable is high, the outputs are held off permitting wire "OR"ing of the three-state outputs of several packages. The use of the enable permits expansion to greater than 32 words.

100000140 100000141 100000142 100000148 100000149 100000215 100000216 100000217 100000218 100000219 100000269 100000270 100000271 100000272 100000273 100000274 100000275 100000276 100000277 100000278 100000279 100000280 100000499 100000500

Pin Configuration



Functional Block Diagram



256-Bit Bipolar Read Only Memory

Logic Diagram/Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

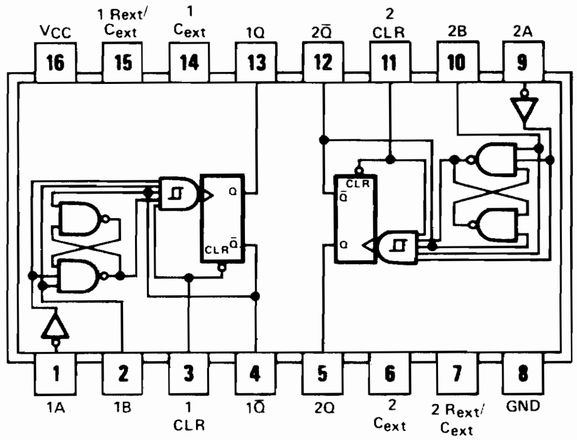
These high speed, electrically programmable, fully decoded TTL bipolar 256-bit read only memories are organized as 32 words by 8 bits.

Memory expansion is simple; three-state outputs are provided on the 100000215; uncommitted collector outputs are provided on all other devices. Each device has on-chip address decoding and chip enable. The memory is fabricated with all logic level zeroes(low); logic level ones (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

100000502

Dual Monostable Multivibrators w/Schmitt-Trigger Inputs

Pin Configuration



Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔

Also see description and switching characteristics

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⊓ = one high-level pulse
⊔ = one low-level pulse
X = irrelevant

The 100000 502 is a monolithic dual multivibrator and features a negative-transition-triggered input and a positive-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

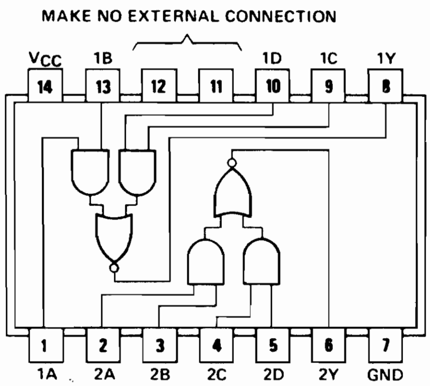
Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With Rext = 2kΩ and C_{ext} = 0, an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

100000383 100000504

Dual 2-Wide 2-Input AND-OR- INVERT Gates

Pin Configuration



Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

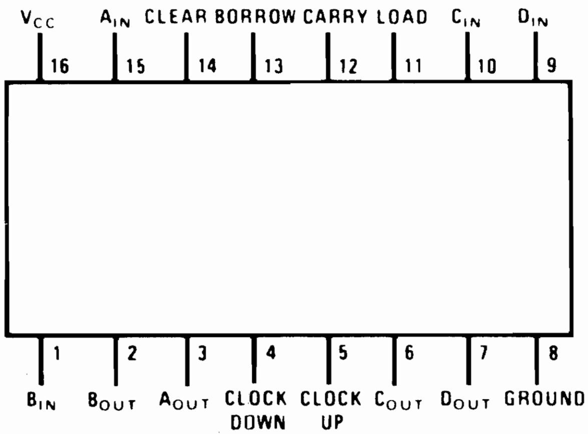
Positive logic: $Y=\overline{AB+CD}$

Note: 100000504 is a Schottky device.

REV. 03

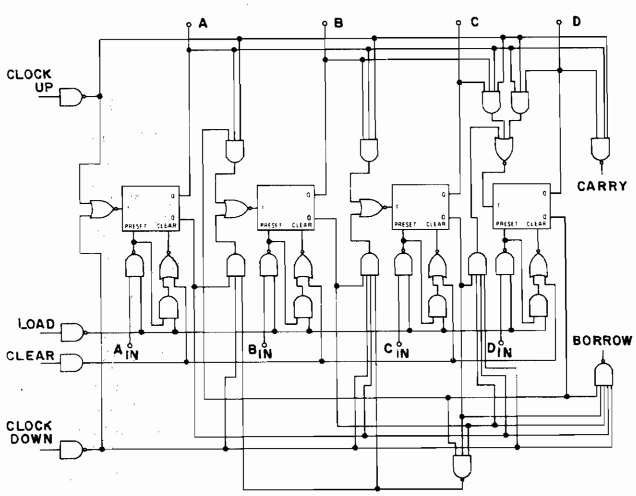
100000508

Pin Configuration



TOP VIEW

Logic Diagram



Up / Down Decade Counter

Pin Designstions

V_{CC} = Pin 16

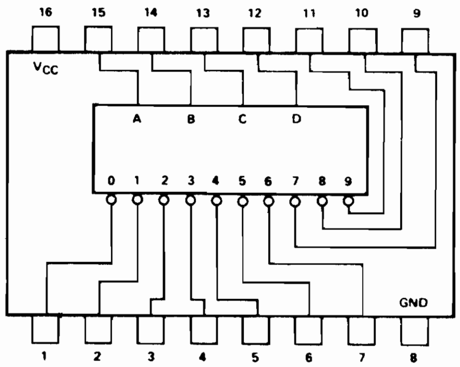
Gnd = Pin 8

The 100000508 is a TTL, compatible, up-down decade counter which is capable of being preset to any number from 0 through 9. A load input controls the asynchronous entry of these numbers, and sets all outputs to appropriate state.

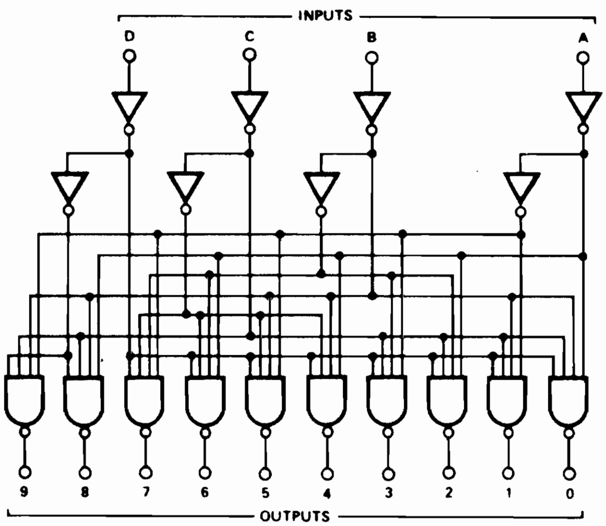
Counting is performed through two clock lines- one controlling the count in the up direction, and the other in the down direction. Two outputs, Borrow and Carry, are connected to the clock inputs of subsequent counters to provide for counting to numbers greater than 9. The counter is synchronous by itself, and "semi-synchronous" (two gate delays between stages) when cascaded.

100000509

Pin Configuration



Logic Diagram



BCD to Decimal Decoder

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

Truth Table

INPUT

D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Truth Table

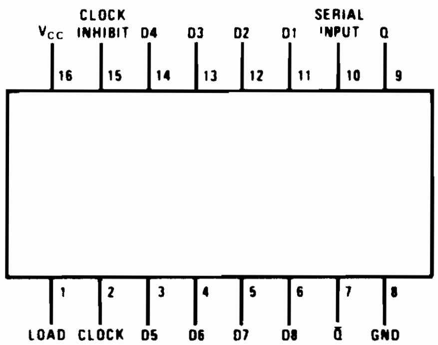
DECIMAL OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

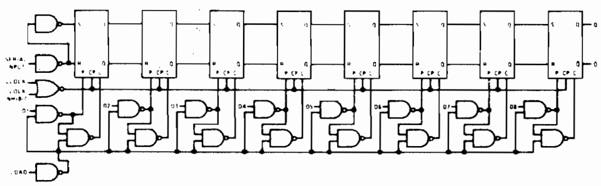
The 100000509 BCD-to-Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion applications. The 100000509 decodes a four bit BCD number to one of ten outputs.

100000510

Pin Configuration



Logic and Connection Diagram



8-Bit Parallel-In Serial-Out Shift Register

Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

The 100000510 utilizes compatible TTL circuitry to provide an eight-bit parallel-in serial-out shift register designed to operate at frequencies of 20MHz. The device also features gating to inhibit clocking, parallel load control, and both Q and $\bar{Q}$ outputs from the last flip-flop for added flexibility.

NOTES:

1. The Clock Inhibit input, when in the logical "1" state, will inhibit the Clock. It must be in the logical "0" state for clocking to occur.

   There is no difference between the Clock Input and the Clock Inhibit input. Their functions may be reversed if ease of layouts results.

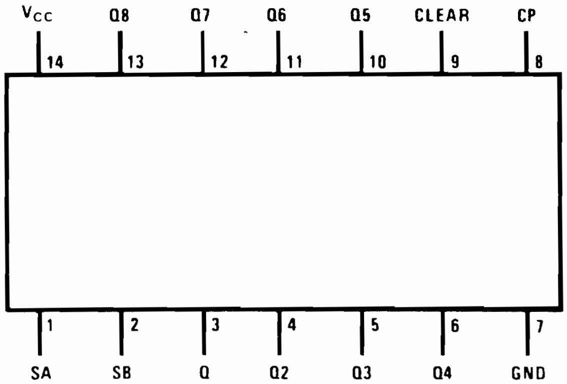
2. Clocking occurs on the positive-going transition of the Clock input.

3. Data on the D1 through D8 inputs will be entered on the negative-going transition of the Load input. This information is entered independent of the state of the Clock, Clock Inhibit, or Serial Input lines. Information on these parallel inputs may be changed while the Load line is enabled thus changing the information in the register.

4. The logic level applied to the Serial Input is entered into the first flip-flop when the register is clocked.

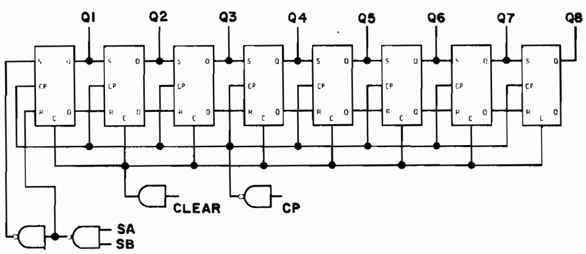
100000511

Pin Configuration



TOP VIEW

Logic and Connection Diagram



8-Bit Serial-In Parallel-Out Shift Register

Pin Designations

V_{CC} = Pin 14

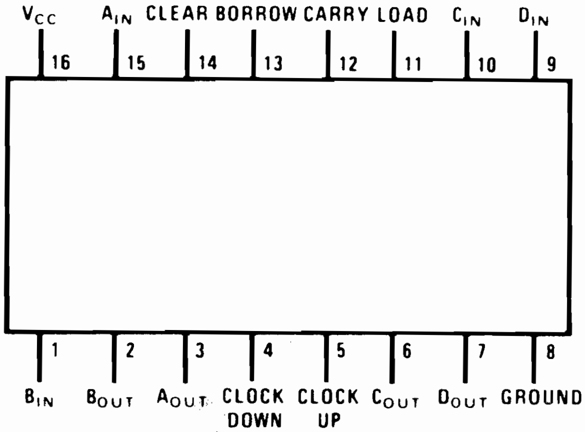
Gnd = Pin 7

The 100000511 utilizes compatible TTL circuitry to provide an eight-bit serial-in parallel-out shift register designed to operate at frequencies of 20MHz. Other features include gated serial inputs for strobe capability and a clear input which, when taken to a logical 0, asynchronously sets all flip-flops to the logical 0 state. Because the flip-flops are R-S instead of J-K, input information may be changed immediately prior to the triggering edge of the clock waveform. Logical 1 levels on SA and SB enter logical 1's into the shift register. Clocking occurs on the positive-going edge of the clock pulse.

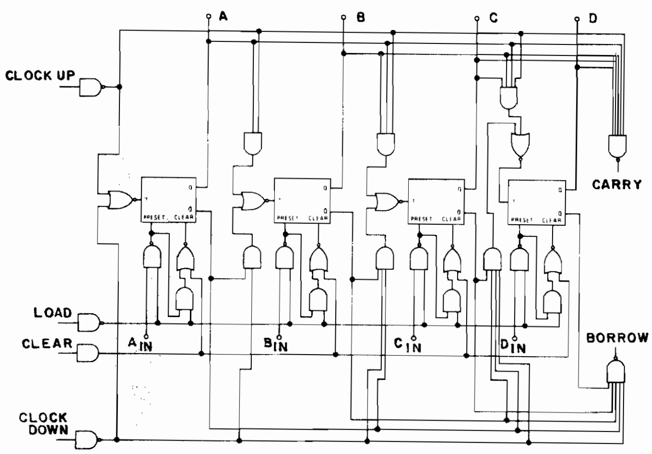
100000512

Up/Down Binary Counter

Pin Configuration



Logic Diagrams



Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

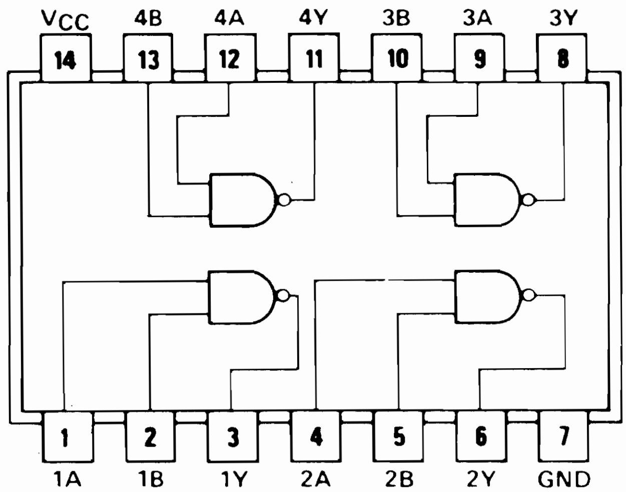
The 100000512 is a TTL compatible, up-down binary counter which is capable of being preset to any number from 0 through 15. A load input controls the asynchronous entry of these numbers, and sets all outputs to appropriate state.

The DM7563/DM8563 is a TTL, Series 54/74 compatible, up-down binary counter which is capable of being preset to any number from 0 through 15. A load input controls the asynchronous entry of these numbers, and sets all outputs to appropriate state.

Counting is performed through two clock lines-one controlling the count in the up direction, and the other in the down direction. Two outputs, Borrow and Carry, are connected to the clock inputs of subsequent counters to provide for counting to numbers greater than 15. The counter is synchronous by itself, and "semi-synchronous" (two gate delays between stages) when cascaded.

100000158 100000340 100000515

Pin Configuration



Quadruple 2-Input Positive-NAND Gate

Logic Diagram/Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Positive logic: $Y = \overline{AB}$

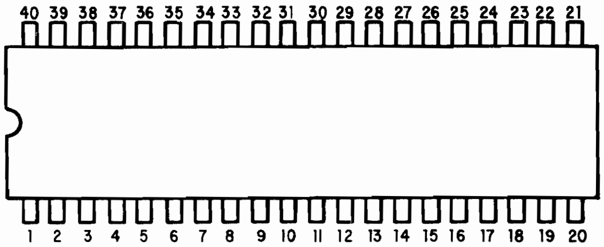
Note: The 100000158 is a Schottky device.

REV. 03

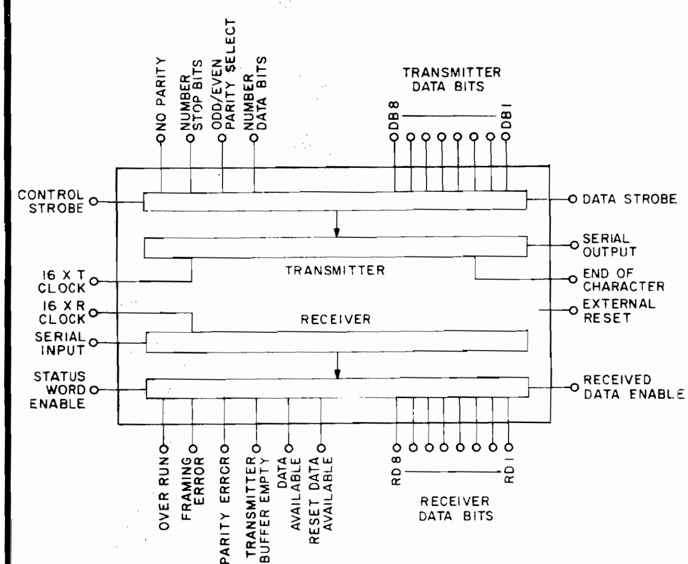
100000130 100000536

Asynchronous Receiver/Transmitter

Pin Configuration



Block Diagram



The Asynchronous Receiver/Transmitter is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits and either odd/even parity or no parity. The baud rate (bits per word), parity mode and the number of stop bits are externally selectable.

Description of Pin Functions

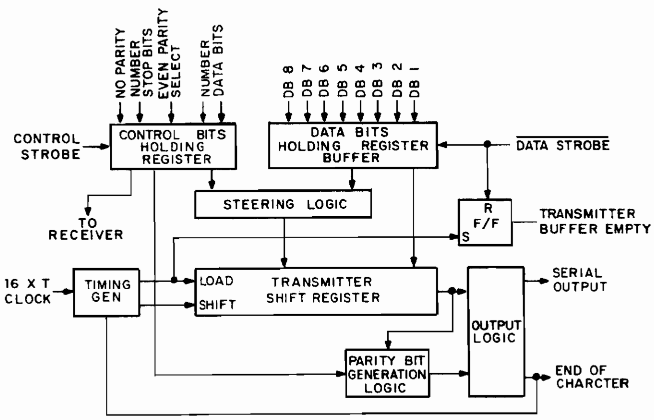
Pin No.	Name	Symbol	Function
1	V_{cc} Power Supply	V_{cc}	+5V Supply
2	V_{gg} Power Supply	V_{gg}	-12V Supply
3	Ground	V_{gr}	Ground
4	Received Data Enable	$\overline{RDE}$	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits	RD8-RD1	These are the 8 data output lines. Received characters are right justified, the LSB always appears on RD1. These lines have tri-state outputs: i.e., they have the normal TTL output characteristics when RDE is "0" and a high impedance state when RDE is "1". Thus, the data output lines can be bus structure oriented.
13	Receive Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected POE.
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit.
15	Over-Run	OR	This line goes to a logic "1" if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver holding register.
16	Status Word Enable	$\overline{SWE}$	A logic "0" on this line places the status word bits (PE, FE, OR, DA, TBMT) onto the output lines. These are tri-state also.
17	Receiver Clock	RCP	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	Reset Data Available	$\overline{RDA}$	A logic "0" will reset the DA line.
19	Receive Data Available	DA	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register.
20	Serial Input	SI	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception.
21	External Reset	XR	Resets all registers. Sets SO, EOC, and TBMT to a logic "1".
22	Transmitter Buffer Empty	TBMT	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character.
23	Data Strobe	$\overline{DS}$	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS.
24	End of Character	EOC	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character.
25	Serial Output	SO	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted.

Continued ....

100000130 100000536

Continued

Transmitter Block Diagram

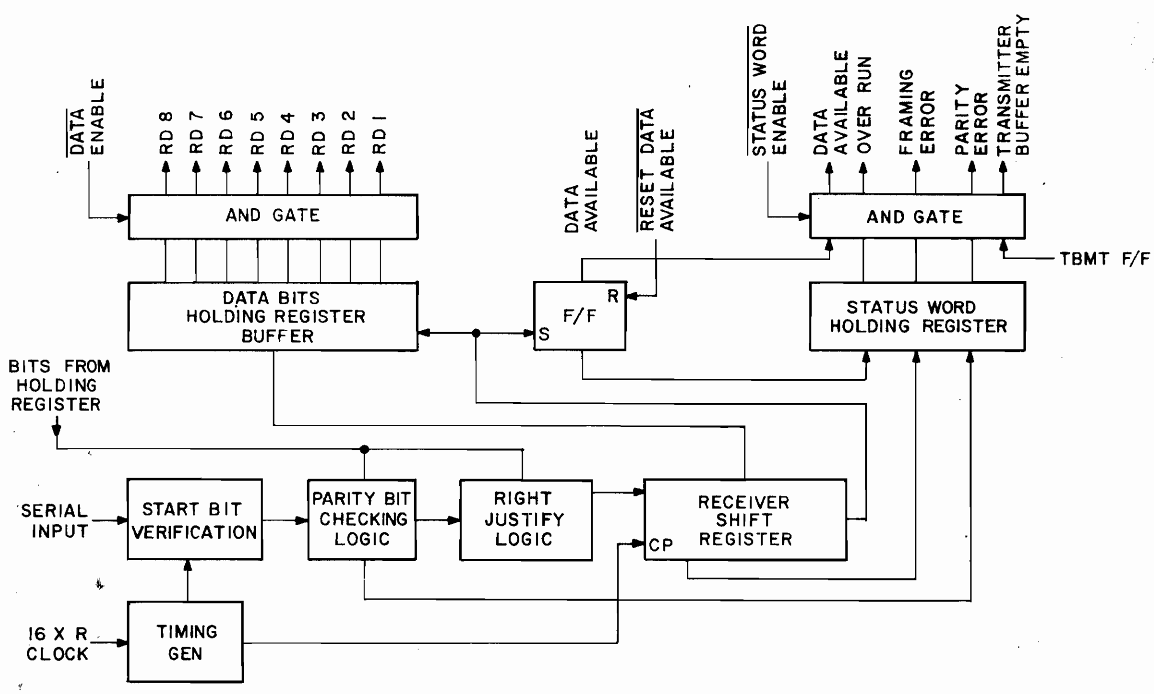


Description of Pin Functions (Continued)

Pin No.	Name	Symbol	Function
26-33	Data Bit Inputs	DB1-DB8	There are up to 8 data bit input lines available.
34	Control Strobe	CS	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity	NP	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits	TSB	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Bits Character	NB2, NB1	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits character. NB1 NB2 Bits Character 0 0 5 1 0 6 0 1 7 1 1 8
39	Odd Even Parity	EPS	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock Line	TCP	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

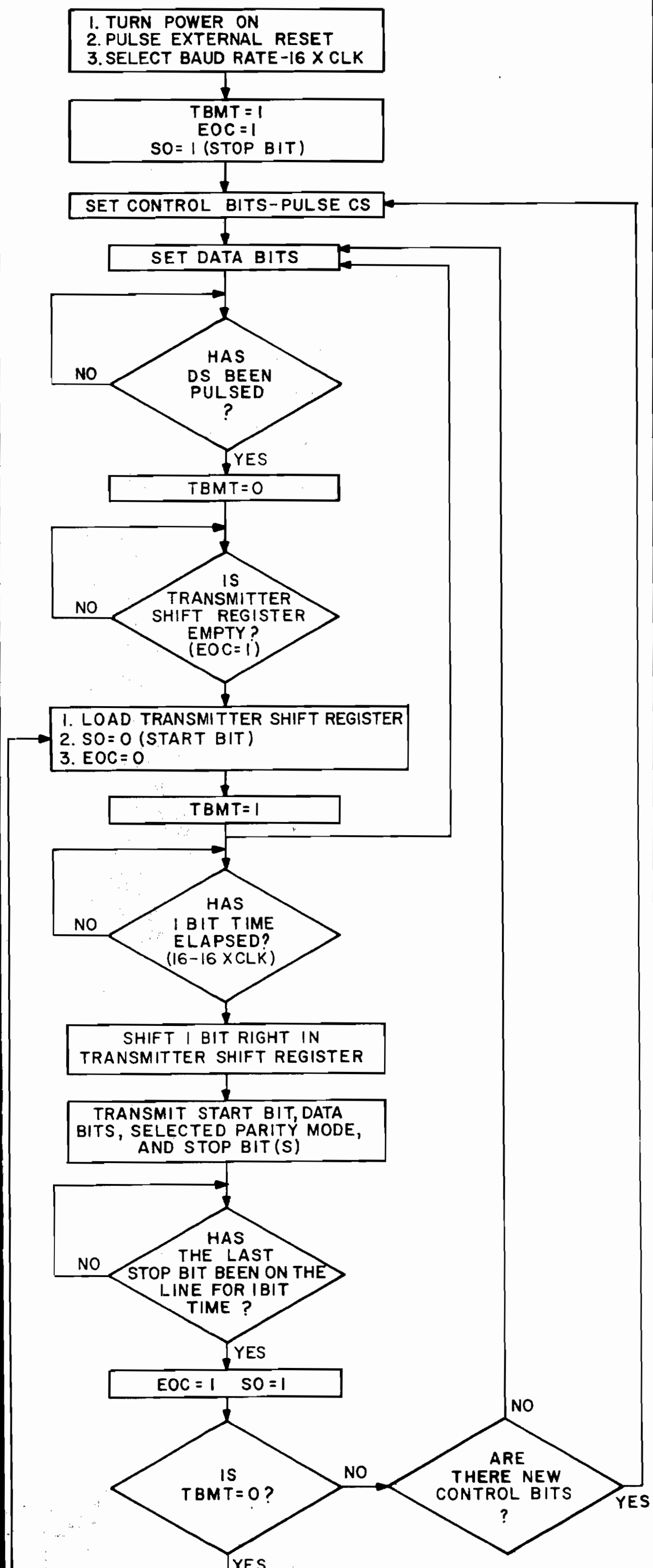
Continued....

Receiver Block Diagram



100000130 100000536

Continued



Transmitter Operation

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBMT, EOC and SO to logic "1" (line is marking).

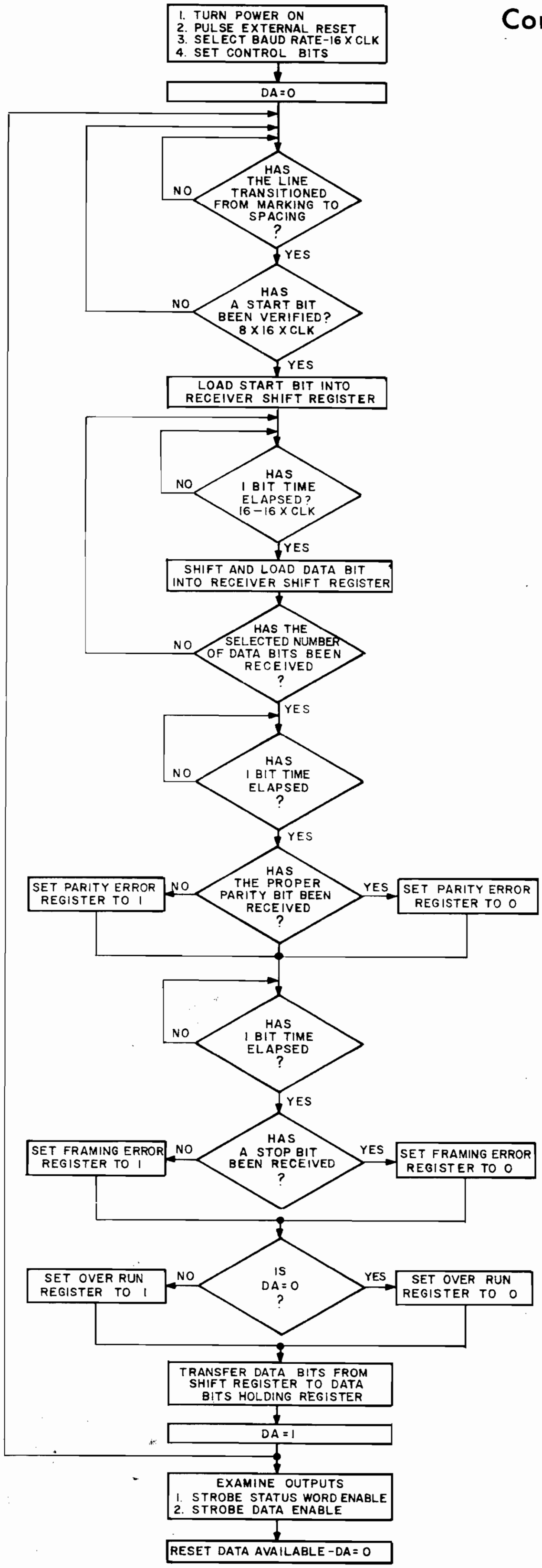
After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once data strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering, (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously mentioned.

Continued....

100000130 100000536

Continued



Receiver Operation

Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DA) to a logic "0".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16X clock is in a logic "1" state, the bit time for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip-flop and/or the framing error flip-flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditioning set to a logic "0".

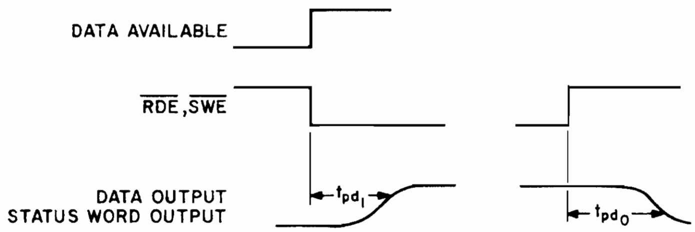
Once a full character is received, internal logic looks at the data available (DA) signal to determine if data has been read out. If the DA signal is at a logic "1" the receiver will assume data has not been read out and the overrun flip-flop of the status word holding register will be set to a logic "1". If the DA signal is at a logic "0" the receiver will assume that data has been read out. After DA goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

Continued....

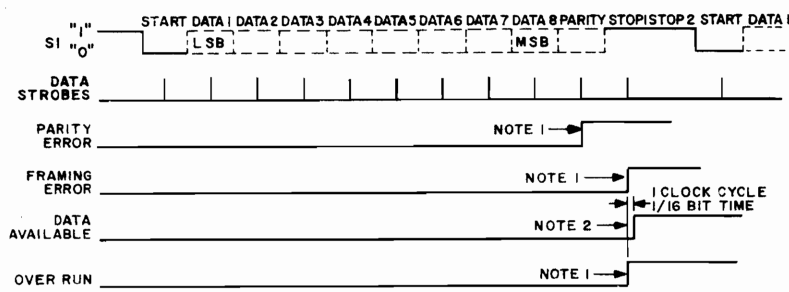
100000130 100000536

Continued

Receiver Propagation Delay Timing Diagram



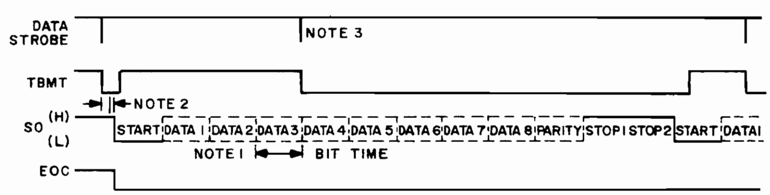
Receiver Timing Diagram



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE DETECTED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGH JUSTIFIED*; THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

Transmitter Timing Diagram



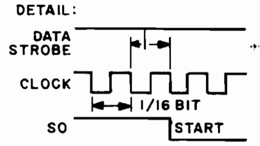
NOTE: TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1.

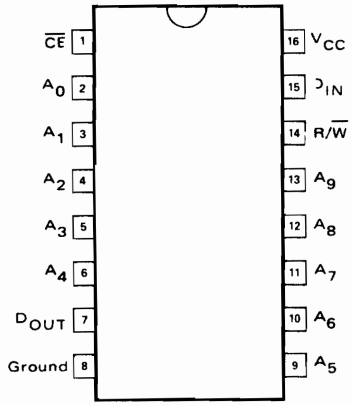
DETAIL:



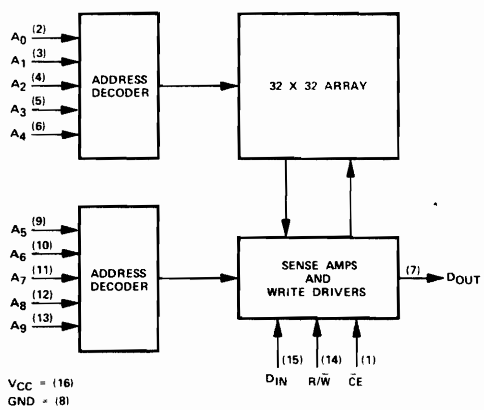
100000465

1024 X 1 Bit Bipolar RAM, Open Collector

Pin Configuration



Block Diagram



Pin Designations

V_{CC} = Pin 16
Pin = Pin 8

The 100000465 is a high speed 1024-bit random access memory organized as 1024 words X 1 bit. It requires a single +5 volts power supply and features very low current PNP input structures. It is fully TTL compatible, and includes on-chip decoding and a chip enable input for ease of memory expansion.

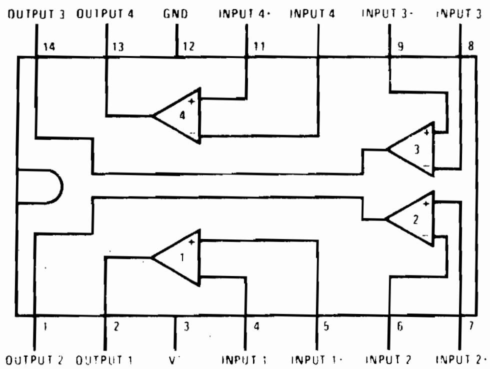
Truth Table

$\overline{C}_E$	$R/\overline{W}$	D_I	MODE	OUTPUT
0	0	0	Write	High
0	0	1	Write	High
0	1	X	Read	Data
1	X	X	Chip Disabled	1

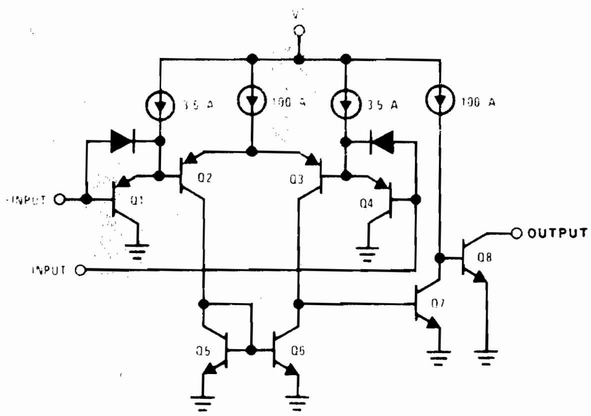
X= Don't care.

100000470

Pin Configuration



Schematic



Voltage Comparator

Pin Designations

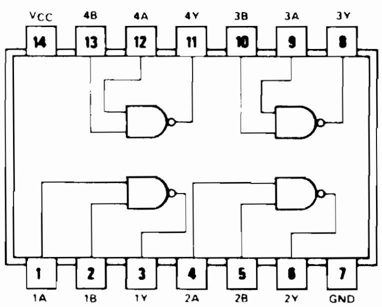
V+ = Pin 3

Gnd = Pin 12

The 100000470 operates from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. The input common-mode voltage range includes ground, even though operated from a single power supply voltage.

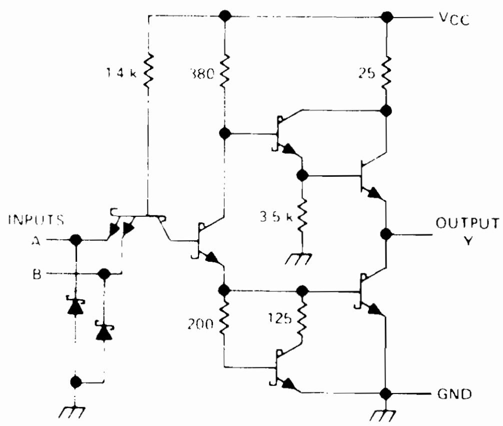
100000472

Pin Configuration



positive logic: $Y = \overline{AB}$

Schematic



Quadruple 2- Input Positive NAND Gate

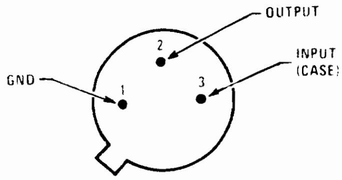
Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

REV. 03

100000484

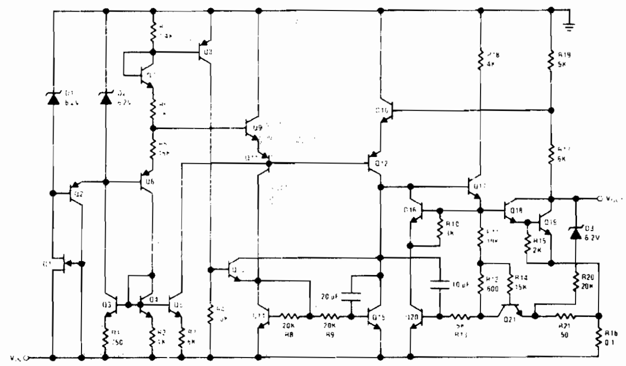
Pin Configuration



BOTTOM VIEW

Schematic

-5V & -5.2V

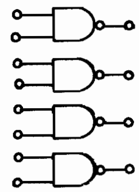


Three Terminal Negative Regulator

The 100000484 is a three-terminal negative regulator with a fixed output voltage of -5V. This device needs only one external component - a compensation capacitor at the output. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

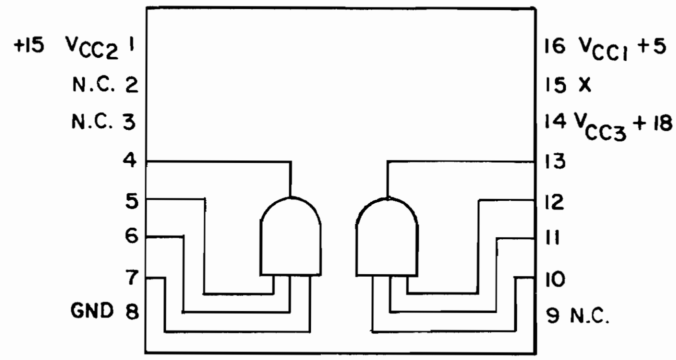
100000487

MOS Clock Driver



100000505

Clock Driver

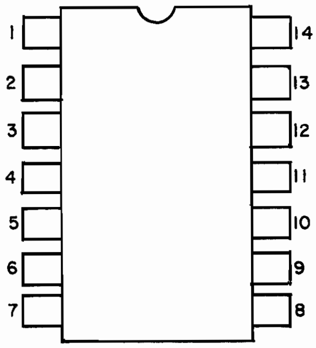


REV. 03

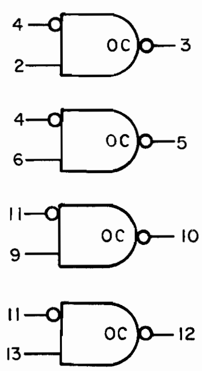
100000506

Sense Amplifier

Pin Configuration



Logic Diagram



-5V—Pin 8
+5—Pin 1 & 14
Gnd—Pin 7

Pin Designations

V+ = Pin 1 & 14

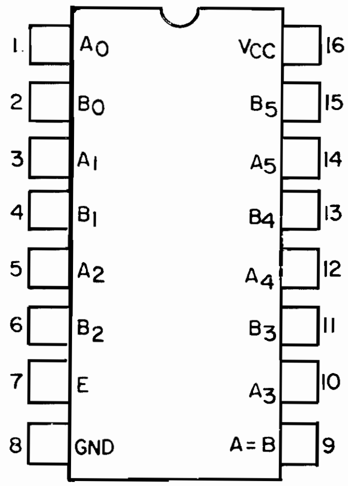
V - = Pin 8

Gnd = Pin 7

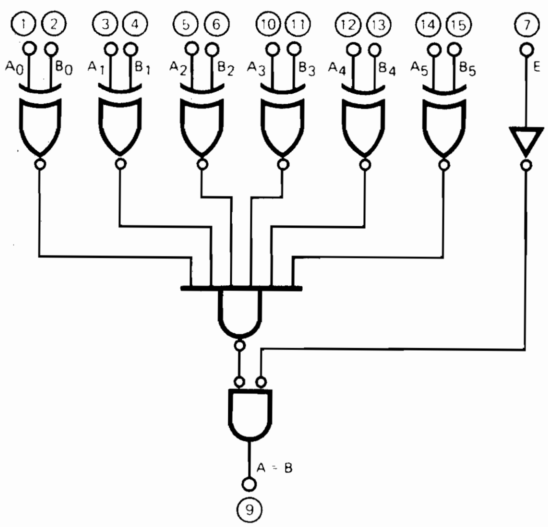
REV. 03

100000540

Pin Configuration



Logic Diagram



High-Speed 6-Bit Identity Comparitor

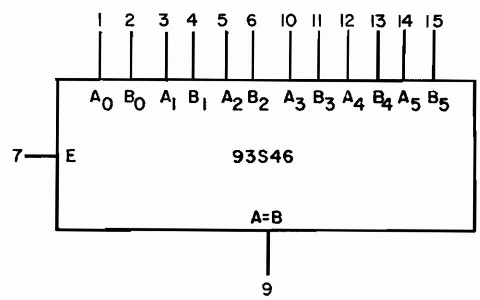
Pin Designations

V_{CC} = Pin 16

Gnd = Pin 8

The 100000540 is a very high speed 6-Bit Identity Comparator. The device compares two words of up to 6-bits and indicates identity in less than 12 ns. It is easily expandable to any word length by using either serial or parallel expansion techniques. When the Enable Input (E) is LOW, it forces the output LOW. The device is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL product families.

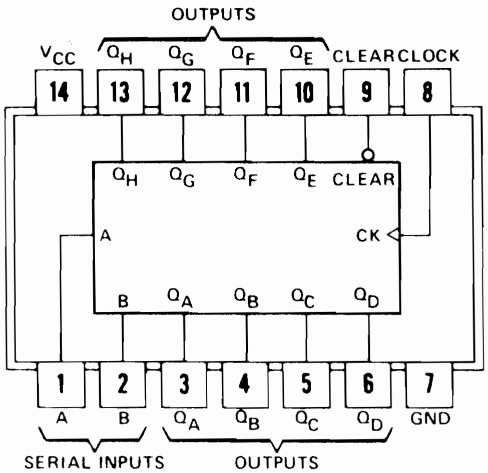
Logic Symbol



REV. 03

100000541

Pin Configuration



Positive Logic : See Truth Table

8-Bit Parallel-Out Serial Shift Registers

Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

Truth Table

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B ...	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

Notes:

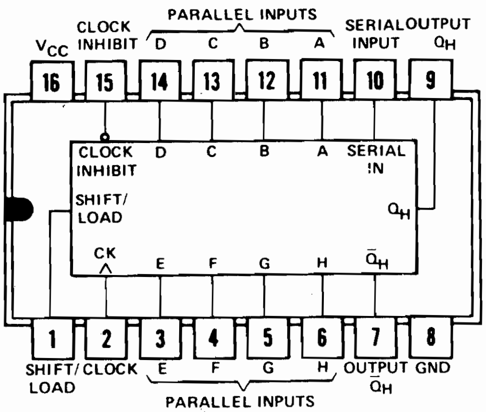
H = high level (steady state),
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

The 100000541 features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the set-up requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

100000542

Pin Configuration



Parallel-Load 8-Bit Shift Register

Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

Truth Table

INPUTS					INTERNAL OUTPUTS		OUTPUT Q_H
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Notes:

H = high level (steady state),
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a. . . h = the level of steady-state input at inputs A thru H, respectively.

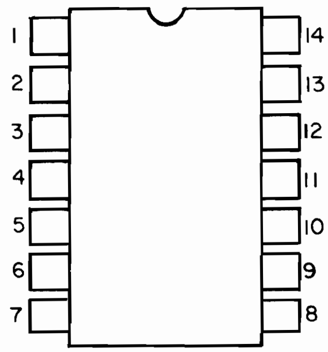
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn}, = the level of Q_A, or Q_G, respectively, before the most recent ↑ transition of the clock.

The 100000542 is an 8-bit serial shift register which shifts the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift/load input. This register also features gated clock inputs and complementary outputs from the eighth bit.

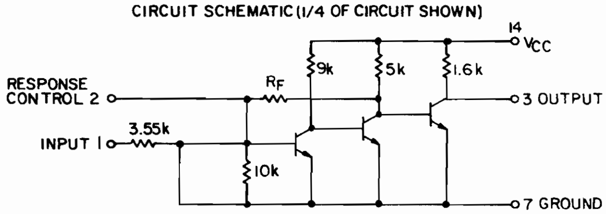
100000545

Pin Configuration



Schematic

CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



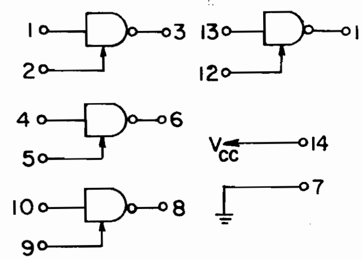
Quad Line Receiver

Pin Designations

V_{CC} = Pin 14
Gnd = Pin 7

The 100000545 is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

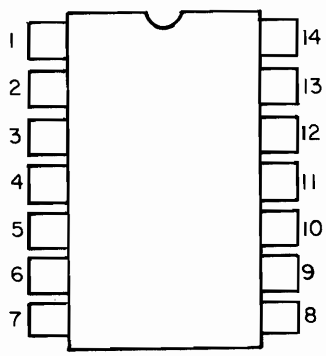
LOGIC DIAGRAM



100000546

Quad MDTL Line Driver

Pin Configuration



Pin Designations

V + = Pin 14

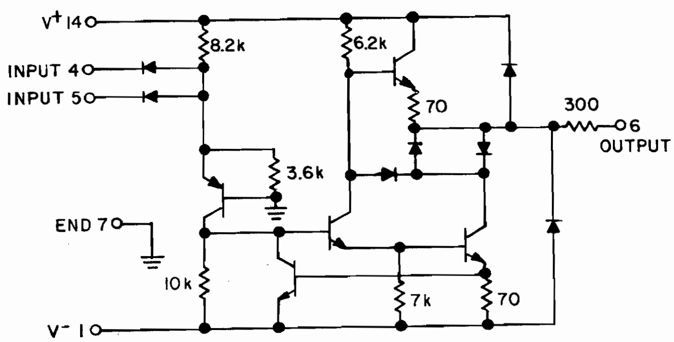
V - = Pin 1

Gnd = Pin 7

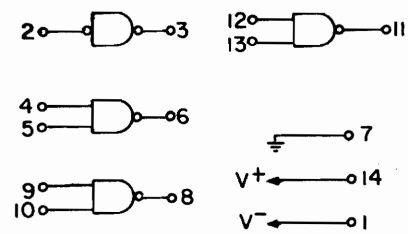
The 100000546 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

Schematic

1/4 OF CIRCUIT SHOWN



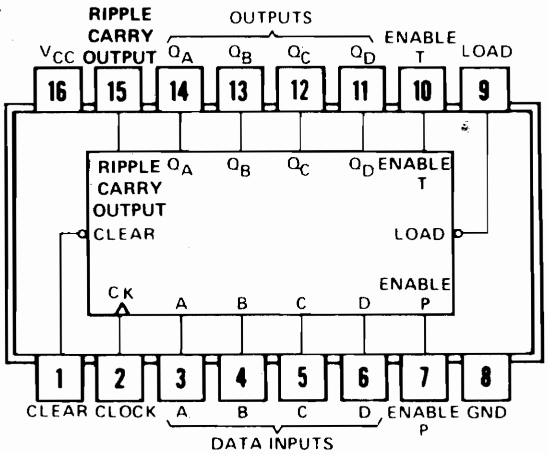
Logic Diagram



REV. 03

100000581

Pin Configuration



Synchronous 4-Bit Counter

Pin Designations

V_{CC} = Pin 16
Gnd = Pin 8

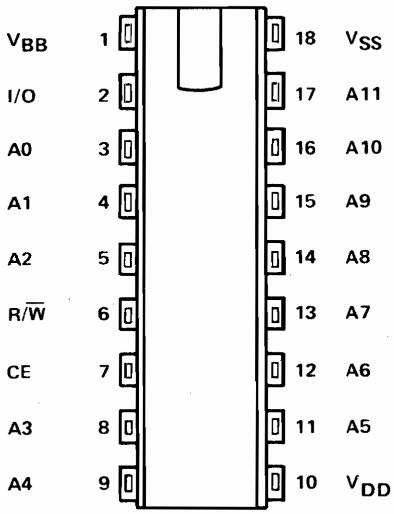
Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

REV. 03

100000590

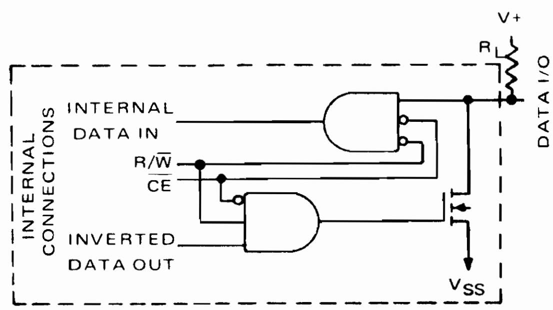
Pin Configuration



4096-Bit Dynamic Random Access Memory

All inputs except the chip-enable are fully TTL-compatible and require no pull-up resistors. The TTL-compatible open-drain buffer is guaranteed to drive 1 TTL gate. The low capacitance of the address and control inputs precludes the need for specialized drivers. The 100000590 uses only one clock (chip-enable) to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers. The data input and output are multiplexed to facilitate compatibility with a common bus system. A 12 line address is available, which minimizes external control logic and optimizes system performance.

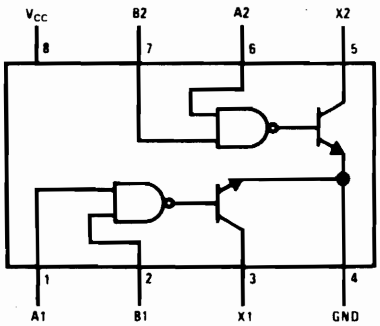
Functional Block Diagram



REV. 03

100000625

Pin Configuration



100000625

Dual Peripheral Driver

V_{CC} = Pin 8
Gnd = Pin 4

Truth Table

100000625

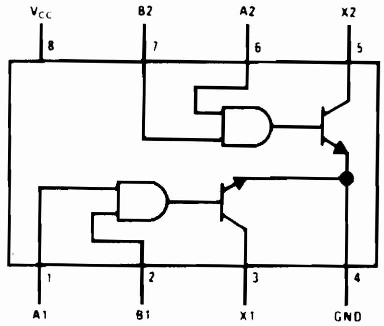
Positive logic: AB=X

A	B	Output X*
0	0	0
1	0	0
0	1	0
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000626

Pin Configuration



100000626

Dual Peripheral Driver

Truth Table

100000626

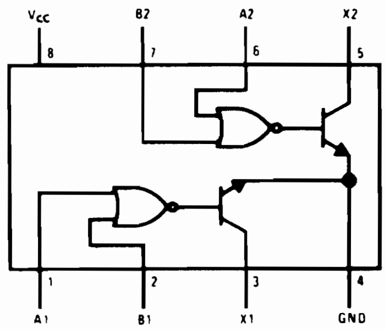
Positive logic: $\overline{AB}$=X

A	B	Output X*
0	0	1
1	0	1
0	1	1
1	1	0

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

100000627

Pin Configuration



100000627

Dual Peripheral Driver

Truth Table

100000627

Positive logic: A + B = X

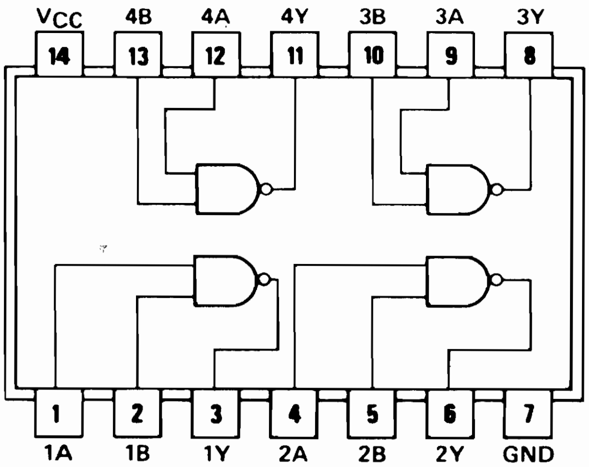
A	B	Output X*
0	0	0
1	0	1
0	1	1
1	1	1

*"0" Output $\leq$ 0.7V
"1" Output $\leq$ 100μA

REV. 03

100000630

Pin Configuration



Quadruple 2-Input Positive-NAND Buffer With Open-Collector Outputs

Logic Diagram/Pin Designations

V_{CC} = Pin 14

Gnd = Pin 7

Positive logic: $Y = \overline{AB}$

REV. 03

PART NUMBER	REV	DESCRIPTION
101-000001-	00	XISTOR 2N3724
101-000002-	00	DIODE CD81148/ FDH600/ WG115/ WG117
101-000003-	00	XISTOR 2N4125
101-000004-	00	XISTOR 2N4441
101-000006-	00	XISTOR 2N4922
101-000013-	00	XISTOR MK20
101-000015-	00	XISTOR 2N3725
101-000016-	00	XISTOR 2N4123
101-000017-	00	DIODE 1N5231
101-000018-	00	XISTOR 2N4918
101-000019-	00	XISTOR 2N5302
101-000021-	00	XISTOR 2N3715
101-000022-	00	DIODE 1N4997
101-000023-	00	DIODE BRIDGE MDA 962-1
101-000024-	00	DIODE MDA 950-1
101-000026-	00	DIODE 1N3879R
101-000027-	00	DIODE 1N5231 20%
101-000028-	00	DIODE 1N5240
101-000031-	00	DIODE ZENER 1N5248B 18V 5%
101-000032-	00	DIODE 1N5228B
101-000036-	00	XISTOR 2N5301 SEE 101000019
101-000038-	00	XISTOR 40526/ 40691 TRIAC
101-000039-	[illegible]	XISTOR SC245B TRIAC
101-000040-	00	FUSR7723393
101-000045-	00	XISTOR MPS 3646, 2N3646, SE3646
101-000046-	00	XISTOR TZ8065
101-000048-	00	DIODE 1N5252B
101-000049-	00	DIODE 1N5243B
101-000050-	00	DIODE CD332864/ .5N5/ .1ZS1 1%
101-000051-	00	XISTOR MPS3640
101-000052-	00	XISTOR 2N4403
101-000058-	00	DIODE 1N5250B 20V 1%
101-000059-	00	XISTOR 2N3789/ 2N3791
101-000061-	00	XISTOR 2N4919
101-000062-	01	XISTOR DG5022
101-000063-	00	XISTOR 2N4399 PNP PWR
101-000064-	00	XISTOR D43C5 PNP
101-000065-	00	DIODE 1N3899R 20AMP
101-000066-	00	DIODE MDA 970-1FW BRIDGE
101-000067-	00	DIODE ZENER 1N5234B 6.2V
101-000068-	00	DIODE MDA 962A-1
101-000069-	00	DIODE 1N5235B/ 1N754A GLASS
101-000070-	00	XISTOR 2N4400
101-000071-	00	DIODE ZENER 1N5251B 22V 5%
101-000072-	00	DIODE 1N5252B/ .5M24ZSE 2%
101-000073-	00	XISTOR TIP 34
101-000074-	00	XISTOR TIP 36 PNP
101-000075-	00	DIODE 1N4001
101-000076-	00	DIODE L209 LED LIGHT-ADMITTING
101-000077-	00	XISTOR TIP 31 NPN
101-000078-	00	XISTOR TIP 36
101-000079-	00	XISTOR 40668
101-000080-	00	DIODE 1N3908R
101-000081-	00	DIODE 1N5348B
101-000082-	00	XISTOR GED 45C5
101-000083-	00	XISTOR 2N4398
101-000084-	00	DIODE 1N3909R
101-000085-	00	DIODE 1N3469
101-000086-	00	DIODE ZENER 1N5248 18V 10%
101-000087-	00	DIODE ZENER 1N5348 11V
101-000088-	00	XISTOR 2N2646
101-000089-	00	DIODE 1N5241B
101-000090-	00	DIODE 1N5225B
101-000091-	00	RECT BRDG MOTOROLA MDA 990-1
101-000092-	00	DIODE 1N4003
101-000093-	00	DIODE 5245
101-000094-	00	XISTOR MPS A13
101-000095-	00	XISTOR 40662 TRIAC
101-000097-	00	XISTOR CN3566
101-000098-	00	XISTOR 2N6005
101-000099-	00	XISTOR 2N6010
101-000100-	00	DIODE 1N5349
101-000101-	00	MDA 980- BRIDGE RECTIFIER
101-000102-	00	DIODE 1N3889R
101-000103-	00	DIODE 1N5231B ZENER
101-000104-	00	XISTOR TIP 30
101-000105-	00	XISTOR TIP 29
101-000106-	00	XISTOR TIP 35
101-000107-	00	DIODE 40108
101-000108-	00	DIODE 1N4448
101-000109-	00	XISTOR TIP 36B
101-000110-	00	DIODE 1N5242
101-000111-	00	XISTOR TIP 42A W/ INSUL H/W
101-000112-	00	DIODE 1N5341
101-000113-	00	DIODE (SEE 101000002)
101-00011[illegible]	00	DIODE CD4148

PART NUMBER	REV	DESCRIPTION
101-000115-	00	XISTOR TEXAS INST TIP33
101-000117-	00	XISTOR HA2-2055A-5 (SEE 100000244)
101-000118-	00	XISTOR HA1-2625-5 (SEE 100000243)
101-000120-	00	DIODE 1N4004
101-000121-	00	MR 1200 50A SILICON RECTIFIER
101-000122-	00	XISTOR 2N6164
101-000123-	00	XISTOR TIP 29A
101-000124-	00	XISTOR TIP 31A
101-000125-	00	DIODE 1N5347
101-000126-	00	DIODE 1N5355
101-000127-	02	XISTOR PHOTO NPN PLANAR SILICON
101-000128-	00	XISTOR TIP 36A
101-000129-	00	XISTOR 40669
101-000130-	00	XISTOR 40527/ 40692/ L4001,5
101-000131-	00	DIODE 1N3880
101-000132-	02	DIODE NETWORK 4-CD8 (148)
101-000133-	00	RECT MR 1210SL 80A SILICON RECT
101-000134-	00	DIODE ZENER 7.5V 1% .5M7.5ZS1
101-000135-	00	DIODE MR 831 MOTOROLA
101-000136-	00	DIODE 1N5236B
101-000137-	00	XISTOR TIP 141
101-000138-	00	XISTOR TIP 146
101-000139-	00	DIODE 1N4735
101-000140-	00	XISTOR 2N4393
101-000141-	00	DIODE ZENER 1N5239B
101-000142-	00	DIODE RECTIFIER 1N4933 MOTOROLA
101-000143-	00	DIODE ZENER 1N5347B 10V 5W +5-5%
101-000144-	00	DIODE ZENER 1N5238B 8.7V 5%
101-000145-	00	DIODE 1N5259
101-000146-	00	DIODE 1N4947
101-000147-	00	DIODE 1N5438B
101-000148-	00	DIODE 1N4934
101-000149-	00	DIODE ZENER 1N4754
101-000150-	00	DIODE ZENER 1N5229B
101-000151-	00	DIODE MLED 500
101-000152-	00	TRIAC T6411D
101-000153-	00	XISTOR TIP 35A
101-000154-	00	XISTOR KE4393 TYPE FET
101-000155-	00	XISTOR 2N4059
101-000156-	00	DIODE LED RT ANGLE (HP#5082-4415)
101-000157-	00	XISTOR TIP 48
101-000158-	00	XISTOR MPS A-42
101-000159-	00	XISTOR MPS A-92
101-000160-	00	XISTOR 2N4888
101-000161-	00	DIODE 1N4077 1000V
101-000162-	00	DIODE 1N5223
101-000163-	00	DIODE ZENER 1N5342B
101-000164-	00	XISTOR MJE 1100
101-000165-	00	TRIAC 40663/ T6411D
101-000166-	00	XISTOR PWR PNP EP1281
101-000167-	00	XISTOR PWR NPN EP1278
101-000168-	00	XISTOR D45H4 PNP
101-000169-	00	XISTOR TA8327 PNP
101-000170-	00	XISTOR NJE 2955 PNP
101-000171-	00	XISTOR RCA 31 NPN
101-000172-	00	XISTOR D44C5 NPN
101-000173-	00	XISTOR 2N6122 NPN
101-000174-	00	XISTOR 2N6125 NPN
101-000175-	00	XISTOR D45H7 PNP
101-000176-	00	XISTOR 2N6133 PNP
101-000177-	00	DIODE 1N5343B ZENER
101-000178-	00	XISTOR 2N6126 PNP/ TIP 42B/ 42C
101-000179-	00	XISTOR D44H7 NPN
101-000180-	00	XISTOR 2N5883 PNP
101-000181-	00	XISTOR 2N3772 PNP
101-000182-	00	XISTOR EP1285 NPN
101-000183-	00	XISTOR 2N6129 NPN
101-000184-	00	XISTOR 2N5987 PNP
101-000185-	00	DIODE ZENER 1N5221B
101-000186-	00	DIODE ZENER 1N5222B
101-000187-	00	DIODE ZENER 1N5223B
101-000188-	00	DIODE ZENER 1N5224B
101-000189-	00	DIODE ZENER 1N5226B
101-000190-	00	DIODE ZENER 1N5227B
101-000191-	00	DIODE ZENER 1N5230B
101-000192-	00	DIODE ZENER 1N5232B
101-000193-	00	DIODE ZENER 1N5233B
101-000194-	00	DIODE ZENER 1N5237B
101-000195-	00	DIODE ZENER 1N5240B
101-000196-	00	DIODE ZENER 1N5242B
101-000197-	00	DIODE ZENER 1N5244B
101-000198-	00	DIODE ZENER 1N5245B
101-000199-	00	XISTOR TIP 41B NPN PWR
101-000200-	00	XISTOR RCA 41B NPN PWR
101-000201-	00	XISTOR 2N6131 NPN PWR
101-000202-	00	XISTOR RCA 42A PNP PWR

PART NUMBER	REV	DESCRIPTION
101-000203-	00	XISTOR 2N3640
101-000204-	00	XISTOR BF 338
101-000205-	00	XISTOR BDY 95
101-000206-	00	XISTOR PHOTO OP640
101-000207-	00	DIODE ZENER 9<1V 5W +5% 1N5346B
101-000208-	00	DIODE TIL209A (LED) LT ADMTG
101-000209-	00	XISTOR 2N3906
101-000210-	00	XISTOR 2N3904
101-000211-	00	DIODE 1N5246B
101-000212-	00	XISTOR 2N4442
101-000213-	00	XISTOR TD-101 NPN
101-000214-	00	XISTOR 2N2219 NPN
101-000215-	00	XISTOR 2N3053 PNP
101-000216-	00	XISTOR 2N3055 NPN
101-000217-	00	XISTOR 2N4037 PNP
101-000218-	00	XISTOR MPS-U51 NPN
101-000219-	00	XISTOR 2N3771 NPN
101-000220-	00	DIODE 1N914
101-000221-	00	DIODE 1N752
101-000222-	00	DIODE 1N4736A
101-000223-	00	DIODE 1N3208
101-000224-	00	DIODE 1N5221 USE 101-185
101-000225-	00	DIODE SCR RCA 40654
101-000226-	00	DIODE RECT BRAKE ASSY
101-000227-	00	XISTOR MJE 2955
101-000228-	00	XISTOR MJE 3055
101-000229-	00	DIODE SZ 3V1/2 W1N52
101-000230-	00	XISTOR 2N3643
101-000231-	00	XISTOR 2N5189
101-000232-	00	XISTOR 2N4916
101-000233-	00	XISTOR 2N3644
101-000234-	00	DIODE A14F
101-000235-	00	XISTOR MPS-U01
101-000236-	00	XISTOR MPS-U51 SELECTED
101-000237-	00	DIODE RECT UCC ASR 33
101-000238-	00	XISTOR TTY UCC ASR 33
101-000239-	00	XISTOR TTY
101-000240-	00	XISTOR DG5022
101-000241-	00	XISTOR MDA 980-2 BRIDGE
101-000242-	00	DIODE 5082-2811/2303
101-000243-	00	TRIAC 2N6165
101-000244-	00	XISTOR HAMMER DRIVE
101-000245-	00	XISTOR SPECIAL
101-000246-	00	XISTOR 2N3253
101-000247-	00	XISTOR 2N2904
101-000248-	00	XISTOR 2N2369A
101-000249-	00	XISTOR 2N2894
101-000250-	00	SEE 101000216
101-000251-	00	XISTOR 2N1595
101-000252-	00	XISTOR 2N1597
101-000253-	00	XISTOR 2N683
101-000254-	00	XISTOR 2N5574/5C50D
101-000255-	00	DIODE SPECIAL SELECT
101-000256-	00	DIODE SEE 100000092
101-000257-	00	DIODE 1N752A
101-000258-	00	DIODE 1N757A
101-000259-	00	DIODE 1N965
101-000260-	00	DIODE 1N1192
101-000261-	00	XISTOR 2N4249
101-000262-	00	XISTOR 2N3565
101-000263-	00	DIODE 3A200
101-000264-	00	DIODE 1N5231B
101-000265-	00	DIODE TYPE 125
101-000266-	00	DIODE 1N2069A
101-000267-	00	DIODE 1N4748A
101-000268-	00	DIODE MD8 962A/1
101-000269-	00	XISTOR 2N5190
101-000270-	00	XISTOR 2N5147 2N149 2N6190
101-000271-	00	DIODE TRIAC
101-000272-	00	XISTOR 2N2219A
101-000273-	00	XISTOR 2N3740
101-000274-	00	DIODE 1N823
101-000275-	00	XISTOR MD 2905A
101-000276-	00	XISTOR MD 2219A
101-000277-	00	DIODE 8 ASSY COMMON ANODE
101-000278-	00	DIODE 8 ASSY COMMON CATHODE
101-000279-	00	XISTOR MD 2369
101-000280-	00	XISTOR 2N5683
101-000281-	00	XISTOR 2N5685
101-000282-	00	XISTOR LTIP-145
101-000283-	00	XISTOR TIP-140
101-000284-	00	DIODE RECTIFIER
101-000285-	00	DIODE SILICON SIGNAL
101-000286-	00	DIODE PHOTOVOITAIC
101-000287-	00	XISTOR PWR 2N5884
101-000288-	00	DIODE MDA-970 USE 101-66

PART NUMBER	REV	DESCRIPTION
101-000289-	00	RECT MDA-980-2
101-000290-	00	XISTOR MJE1103
101-000291-	00	XISTOR PHOTO SPECIAL
101-000292-	00	DIODE MDA-952-1
101-000293-	00	XISTOR MM4001
101-000294-	00	XISTOR MM3009
101-000295-	00	XISTOR SEE 101-298
101-000296-	00	XISTOR PN4258A PBP
101-000297-	00	XISTOR MPS 2369
101-000298-	00	XISTOR SPECIAL FOR 2230
101-000299-	00	XISTOR 2N4091
101-000300-	00	DIODE LED TIL-210
101-000301-	00	DIODE 1N3062, TID778, FDN700
101-000302-		DIODE 1N3317
101-000303-		DIODE 1N3305
101-000304-	00	XISTOR OUTLINE READOUT ASSY CTG DISK
101-000305-	00	XISTOR 2N2905A
101-000306-	00	DIODE ZENER 4.9V 1% 500MW
101-000307-		DIODE MDA990-2

PART NUMBER	REV	DESCRIPTION
102-000001-	00	RES 2.70 OHM 1/4W 5%
102-000002-	00	RES 3.00 OHM 1/4W 5%
102-000003-	00	RES 3.30 OHM 1/4W 5%
102-000004-	00	RES 3.60 OHM 1/4W 5%
102-000005-	00	RES 3.90 OHM 1/4W 5%
102-000006-	00	RES 4.30 OHM 1/4W 5%
102-000007-	00	RES 4.70 OHM 1/4W 5%
102-000008-	00	RES 5.10 OHM 1/4W 5%
102-000009-	00	RES 5.60 OHM 1/4W 5%
102-000010-	00	RES 6.20 OHM 1/4W 5%
102-000011-	00	RES 6.80 OHM 1/4W 5%
102-000012-	00	RES 7.50 OHM 1/4W 5%
102-000013-	00	RES 8.20 OHM 1/4W 5%
102-000014-	00	RES 9.10 OHM 1/4W 5%
102-000015-	00	RES 10.00 OHM 1/4W 5%
102-000016-	00	RES 11.00 OHM 1/4W 5%
102-000017-	00	RES 12.00 OHM 1/4W 5%
102-000018-	00	RES 13.00 OHM 1/4W 5%
102-000019-	00	RES 15.00 OHM 1/4W 5%
102-000020-	00	RES 16.00 OHM 1/4W 5%
102-000021-	00	RES 18.00 OHM 1/4W 5%
102-000022-	00	RES 20.00 OHM 1/4W 5%
102-000023-	00	RES 22.00 OHM 1/4W 5%
102-000024-	00	RES 24.00 OHM 1/4W 5%
102-000025-	00	RES 27.00 OHM 1/4W 5%
102-000026-	00	RES 30.00 OHM 1/4W 5%
102-000029-	00	RES 39.00 OHM 1/4W 5%
102-000030-	00	RES 43.00 OHM 1/4W 5%
102-000031-	00	RES 47.00 OHM 1/4W 5%
102-000032-	00	RES 51.00 OHM 1/4W 5%
102-000033-	00	RES 56.00 OHM 1/4W 5%
102-000034-	00	RES 62.00 OHM 1/4W 5%
102-000035-	00	RES 68.00 OHM 1/4W 5%
102-000036-	00	RES 75.00 OHM 1/4W 5%
102-000037-	00	RES 82.00 OHM 1/4W 5%
102-000039-	00	RES 100.00 OHM 1/4W 5%
102-000040-	00	RES 110.00 OHM 1/4W 5%
102-000041-	00	RES 120.00 OHM 1/4W 5%
102-000042-	00	RES 130.00 OHM 1/4W 5%
102-000043-	00	RES 150.00 OHM 1/4W 5%
102-000044-	00	RES 160.00 OHM 1/4W 5%
102-000045-	00	RES 180.00 OHM 1/4W 5%
102-000046-	00	RES 200.00 OHM 1/4W 5%
102-000047-	00	RES 220.00 OHM 1/4W 5%
102-000048-	00	RES 240.00 OHM 1/4W 5%
102-000049-	00	RES 270.00 OHM 1/4W 5%
102-000050-	00	RES 300.00 OHM 1/4W 5%
102-000051-	00	RES 330.00 OHM 1/4W 5%
102-000052-	00	RES 360.00 OHM 1/4W 5%
102-000053-	00	RES 390.00 OHM 1/4W 5%
102-000054-	00	RES 430.00 OHM 1/4W 5%
102-000055-	00	RES 470.00 OHM 1/4W 5%
102-000056-	00	RES 510.00 OHM 1/4W 5%
102-000057-	00	RES 560.00 OHM 1/4W 5%
102-000058-	00	RES 620.00 OHM 1/4W 5%
102-000059-	00	RES 680.00 OHM 1/4W 5%
102-000060-	00	RES 750.00 OHM 1/4W 5%
102-000061-	00	RES 820.00 OHM 1/4W 5%
102-000062-	00	RES 910.00 OHM 1/4W 5%
102-000063-	00	RES 1.00K OHM 1/4W 5%
102-000064-	00	RES 1.10K OHM 1/4W 5%
102-000065-	00	RES 1.20K OHM 1/4W 5%
102-000066-	00	RES 1.30K OHM 1/4W 5%
102-000067-	00	RES 1.50K OHM 1/4W 5%
102-000068-	00	RES 1.60K OHM 1/4W 5%
102-000069-	00	RES 1.80K OHM 1/4W 5%
102-000070-	00	RES 2.00K OHM 1/4W 5%
102-000071-	00	RES 2.20K OHM 1/4W 5%
102-000072-	00	RES 2.40K OHM 1/4W 5%
102-000073-	00	RES 2.70K OHM 1/4W 5%
102-000074-	00	RES 3.00K OHM 1/4W 5%
102-000075-	00	RES 3.30K OHM 1/4W 5%
102-000076-	00	RES 3.60K OHM 1/4W 5%
102-000077-	00	RES 4.30K OHM 1/4W 5%
102-000078-	00	RES 4.70K OHM 1/4W 5%
102-000079-	00	RES 5.10K OHM 1/4W 5%
102-000080-	00	RES 5.60K OHM 1/4W 5%
102-000081-	00	RES 6.20K OHM 1/4W 5%
102-000082-	00	RES 6.80K OHM 1/4W 5%
102-000083-	00	RES 7.50K OHM 1/4W 5%
102-000084-	00	RES 8.20K OHM 1/4W 5%
102-000085-	00	RES 9.10K OHM 1/4W 5%
102-000086-	00	RES 10.00K OHM 1/4W 5%
102-000087-	00	RES 11.00K OHM 1/4W 5%
102-000088-	00	RES 12.00K OHM 1/4W 5%
102-000089-	00	RES 13.00K OHM 1/4W 5%
102-000090-	00	RES 15.00K OHM 1/4W 5%
102-000091-	00	RES 16.00K OHM 1/4W 5%
102-000092-	00	RES 18.00K OHM 1/4W 5%
102-000093-	00	RES 20.00K OHM 1/4W 5%
102-000094-	00	RES 22.00K OHM 1/4W 5%
102-000095-	00	RES 24.00K OHM 1/4W 5%
102-000096-	00	RES 27.00K OHM 1/4W 5%
102-000097-	00	RES 30.00K OHM 1/4W 5%
102-000098-	00	RES 33.00K OHM 1/4W 5%
102-000099-	00	RES 36.00K OHM 1/4W 5%
102-000100-	00	RES 39.00K OHM 1/4W 5%
102-000101-	00	RES 43.00K OHM 1/4W 5%
102-000102-	00	RES 47.00K OHM 1/4W 5%
102-000103-	00	RES 51.00K OHM 1/4W 5%
102-000104-	00	RES 56.00K OHM 1/4W 5%
102-000105-	00	RES 62.00K OHM 1/4W 5%
102-000106-	00	RES 68.00K OHM 1/4W 5%
102-000107-	00	RES 75.00K OHM 1/4W 5%
102-000108-	00	RES 82.00K OHM 1/4W 5%
102-000109-	00	RES 91.00K OHM 1/4W 5%
102-000110-	00	RES 100.00K OHM 1/4W 5%
102-000111-	00	RES 110.00K OHM 1/4W 5%
102-000112-	00	RES 120.00K OHM 1/4W 5%
102-000113-	00	RES 130.00K OHM 1/4W 5%
102-000114-	00	RES 150.00K OHM 1/4W 5%
102-000115-	00	RES 160.00K OHM 1/4W 5%
102-000116-	00	RES 180.00K OHM 1/4W 5%
102-000117-	00	RES 200.00K OHM 1/4W 5%
102-000118-	00	RES 220.00K OHM 1/4W 5%
102-000119-	00	RES 240.00K OHM 1/4W 5%
102-000120-	00	RES 270.00K OHM 1/4W 5%
102-000121-	00	RES 300.00K OHM 1/4W 5%
102-000122-	00	RES 330.00K OHM 1/4W 5%
102-000123-	00	RES 360.00K OHM 1/4W 5%
102-000124-	00	RES 390.00K OHM 1/4W 5%
102-000125-	00	RES 430.00K OHM 1/4W 5%
102-000126-	00	RES 470.00K OHM 1/4W 5%
102-000127-	00	RES 510.00K OHM 1/4W 5%
102-000128-	00	RES 560.00K OHM 1/4W 5%
102-000129-	00	RES 620.00K OHM 1/4W 5%
102-000130-	00	RES 680.00K OHM 1/4W 5%
102-000131-	00	RES 750.00K OHM 1/4W 5%
102-000132-	00	RES 820.00K OHM 1/4W 5%
102-000133-	00	RES 910.00K OHM 1/4W 5%
102-000134-	00	RES 1.00M OHM 1/4W 5%
102-000135-	00	RES 1.10M OHM 1/4W 5%
102-000136-	00	RES 1.20M OHM 1/4W 5%
102-000137-	00	RES 1.30M OHM 1/4W 5%
102-000138-	00	RES 1.50M OHM 1/4W 5%
102-000139-	00	RES 1.60M OHM 1/4W 5%
102-000140-	00	RES 1.80M OHM 1/4W 5%
102-000141-	00	RES 2.00M OHM 1/4W 5%
102-000142-	00	RES 2.20M OHM 1/4W 5%
102-000143-	00	RES 2.40M OHM 1/4W 5%
102-000144-	00	RES 2.70M OHM 1/4W 5%
102-000145-	00	RES 3.00M OHM 1/4W 5%
102-000146-	00	RES 3.30M OHM 1/4W 5%
102-000147-	00	RES 3.60M OHM 1/4W 5%
102-000148-	00	RES 3.90M OHM 1/4W 5%
102-000149-	00	RES 4.30M OHM 1/4W 5%
102-000150-	00	RES 4.70M OHM 1/4W 5%
102-000151-	00	RES 5.10M OHM 1/4W 5%
102-000152-	00	RES 5.60M OHM 1/4W 5%
102-000153-	00	RES 6.20M OHM 1/4W 5%
102-000154-	00	RES 6.80M OHM 1/4W 5%
102-000155-	00	RES 7.50M OHM 1/4W 5%
102-000156-	00	RES 8.20M OHM 1/4W 5%
102-000157-	00	RES 9.10M OHM 1/4W 5%
102-000158-	00	RES 10.00M OHM 1/4W 5%
102-000159-	00	RES 11.00M OHM 1/4W 5%
102-000160-	00	RES 12.00M OHM 1/4W 5%
102-000161-	00	RES 13.00M OHM 1/4W 5%
102-000162-	00	RES 15.00M OHM 1/4W 5%
102-000163-	00	RES 16.00M OHM 1/4W 5%
102-000164-	00	RES 18.00M OHM 1/4W 5%
102-000165-	00	RES 20.00M OHM 1/4W 5%
102-000166-	00	RES 22.00M OHM 1/4W 5%
102-000167-	00	RES 24.00M OHM 1/4W 5%
102-000168-	00	RES 27.00M OHM 1/4W 5%
102-000169-	00	RES 30.00M OHM 1/4W 5%
102-000170-	00	RES 33.00M OHM 1/4W 5%
102-000171-	00	RES 36.00M OHM 1/4W 5%
102-000172-	00	RES 39.00M OHM 1/4W 5%
102-000173-	00	RES 43.00M OHM 1/4W 5%
102-000174-	00	RES 47.00M OHM 1/4W 5%
102-000175-	00	RES 51.00M OHM 1/4W 5%

PART NUMBER	REV	DESCRIPTION
102-000176-	00	RES 56.00M OHM 1/4W 5%
102-000177-	00	RES 62.00M OHM 1/4W 5%
102-000178-	00	RES 68.00M OHM 1/4W 5%
102-000179-	00	RES 75.00M OHM 1/4W 5%
102-000180-	00	RES 82.00M OHM 1/4W 5%
102-000181-	00	RES 91.00M OHM 1/4W 5%
102-000182-	00	RES 100.00M OHM 1/4W 5%
102-000183-	00	RES 5.00 OHM 1/4W 5%
102-000185-	00	RES 150.00 OHM 1/10W 1%
102-000186-	00	RES 17.50 OHM 3W 1%
102-000187-	00	RES 22.50 OHM 3W 1%
102-000188-	00	RES .10 OHM 2W 1%
102-000189-	00	RES 1.00 OHM 3W 5%
102-000190-	00	RES 10.00K OHM 10W %
102-000191-	00	RES 180.00 OHM 2W 5%
102-000192-	00	RES 180.00 OHM 3W 5%
102-000193-	00	RES 330.00 OHM 3W 5%
102-000194-	00	RES 470.00 OHM 3W 5%
102-000195-	00	RES 600.00 OHM 3W 5%
102-000196-	00	RES 1.00 OHM 5W %
102-000197-	00	RES 4.00K OHM 10W %
102-000198-	00	RES 12.00 OHM 1/4W 5%
102-000199-	00	RES NETWORK SUBSTRATE
102-000200-	00	RES . OHM W % THMC
102-000201-	00	RES 3.90K OHM 1/4W 5%
102-000202-	00	RES 15.00 OHM W 1%
102-000203-	00	RES 12.50 OHM W 1%
102-000204-	00	RES 11.00 OHM W 1%
102-000205-	00	RES 14.00 OHM W 1%
102-000206-	00	RES 680.00 OHM 2W
102-000207-	00	RES 95.30 OHM W 1%
102-000208-	00	RES 25.00 OHM W %
102-000209-	00	RES 470.00 OHM 1W 5%
102-000210-	00	RES 1.50K OHM 1/8W 1%
102-000211-	00	RES 1.65K OHM 1/8W 1%
102-000212-	00	RES 1.82K OHM 1/8W 1%
102-000213-	00	RES 2.00K OHM 1/8W 1%
102-000214-	00	RES 2.21K OHM 1/8W 1%
102-000215-	00	RES 15.00K OHM 1/8W 1%
102-000216-	00	RES 1.30K OHM 1/8W 1%
102-000217-	00	RES 200.00 OHM 1/8W 5%
102-000218-	00	RES 240.00 OHM 1/8W 5%
102-000219-	00	RES 330.00 OHM 1/8W 5%
102-000220-	00	RES 390.00 OHM 1/8W 5%
102-000221-	00	POT 2.00K OHM 1W 10%
102-000222-	00	POT 20.00K OHM 1W 10%
102-000223-	00	RES 11.00 OHM W 2%
102-000224-	00	RES 14.00 OHM 1%
102-000225-	00	THM 4" DISC 300 FNWL LA 23W1
102-000226-	00	RES 95.30 OHM 1/2W 1%
102-000227-	00	RES 25.00 OHM 3W 5%
102-000228-	00	RES 8.00 OHM 4W 3%
102-000229-	00	RES 30.00 OHM 3W 1%
102-000230-	00	RES .20 OHM 10W 5%
102-000231-	00	RES .50 OHM 3W 5%
102-000232-	00	RES 4.00 OHM 5W 5%
102-000233-	00	RES 390.00 OHM 1/2W 5%
102-000234-	00	RES 10.00 OHM 1/2W 5%
102-000235-	00	POT 100.00 OHM 1/2W 10%
102-000236-	00	RES 390.00 OHM 3W 5%
102-000237-	00	RES 180.00 OHM 1W 5%
102-000238-	00	RES 11.00 OHM 4W 3%
102-000239-	00	RES 14.00 OHM 3W 1%
102-000240-	00	RES 53.60 OHM 3W 1%
102-000241-	00	RES 10.00K OHM 1/4W 1%
102-000242-	00	RES 3.32K OHM 1/4W 1%
102-000243-	00	RES 12.10K OHM 1/8W 1%
102-000244-	00	RES 5.62K OHM 1/8W 1%
102-000245-	00	THM 5.00K OHM W % THMC
102-000246-	00	RES 17.50 OHM 3W 1%
102-000247-	00	RES 75.00 OHM 3W 1%
102-000248-	00	RES 100.00 OHM 3W 1%
102-000249-	00	RES 10.00 OHM 1/4W 1%
102-000250-	00	RES 6.81K OHM 1/4W 1%
102-000251-	00	RES 1.50 OHM 3W 5% W.W.
102-000252-	00	RES 270.00 OHM 1W 5% CARBON
102-000253-	00	RES 91.00 OHM 1/4W 5% PIH/COR
102-000254-	00	RES 30.00 OHM 1/4W 5%
102-000255-	00	RES 91.00 OHM 1/2W 5%
102-000256-	00	RES 7.87K OHM 1/4W 1%
102-000257-	00	RES 38.00 OHM 3W 1% A-P WOU
102-000258-	00	RES 47.00 1/2W 5%
102-000259-	00	RES 3.60 OHM 1W 5% CARBON
102-000260-	00	RES 50.00 OHM 5W 5%
102-000261-	00	RES 130.00 OHM 1/4W 5% PIHER
102-000262-	00	RES 3.00 OHM 1W 5% CARBON
102-000263-	00	RES 33.00 OHM 1/4W 5% PIHER
102-000264-	00	RES 160.00 OHM 1/4W 5% PIHER O
102-000265-	00	RES 27.00 OHM 1/2W 5% (1/2WR)
102-000266-	00	RES 150.00 OHM 3W 1% A-P WOU
102-000267-	00	RES 220.00 OHM 1/2W 5% CARBON
102-000268-	00	RES 30.00 OHM 1/2W 5%
102-000269-	00	RES 510.00 OHM 1/2W 5% CARBON
102-000270-	00	RES 7.50 OHM 2W 5% O
102-000271-	00	RES 34.00 OHM 1/4W 1%
102-000272-	00	RES .05 OHM 5W 5% W/W
102-000273-	00	RES 470.00 OHM 1/2W 5%
102-000274-	00	RES 1.50 OHM 1/2W 5% CARBON
102-000275-	00	RES 1.50 OHM 20W
102-000276-	00	RES 15.00 OHM 12W
102-000277-	00	RES 50.00 OHM 20W
102-000278-	00	RES DUMMY
102-000279-	00	RES 120-00 OHM 1/2W 5% PIHER/CRNG C5M
102-000280-	00	RES 140.00 OHM 1/2W 2%
102-000281-	00	RES 5.10K OHM 2W 5% CARBON
102-000282-	00	RES 10.00K OHM 2W 5% CARBON
102-000283-	00	RES 1.00K OHM 1/2W 5%
102-000284-	00	POT 5.00K OHM
102-000285-	00	POT 500.00K OHM
102-000286-	00	RES 36.00 OHM TPR 5% PI/C RL20
102-000287-	00	RES 39.00 OHM 1/4W 5% PIHER
102-000288-	00	POT 50.00K OHM 1W 10%
102-000289-	00	RES .10 OHM 10W 5%
102-000290-	00	RES 75.00 OHM 1W 5%
102-000291-	00	RES 0.50 OHM 10W 5%
102-000292-	00	RES 82.00 OHM 1/2W 5%
102-000293-	00	POT 500.00 OHM
102-000294-	00	POT 1.00K OHM 5%
102-000295-	00	POT 10.00K OHM 5%
102-000296-	00	RES 50.00 OHM 50W 5%
102-000297-	00	RES 150.00 OHM 1/8W 1%
102-000298-	00	RES 6.80K OHM 1/8W 1%
102-000300-	00	RES 6.80 OHM 1/2W 5%
102-000301-	00	RES 150.00 OHM 2W 5%
102-000302-	00	RES 12.00 OHM 5W 5%
102-000303-	00	POT 500.00 OHM 1W 10%
102-000304-	00	RES 1.00K OHM 1/4W 1%
102-000305-	00	POT 10.00K OHM 3/4W
102-000306-	00	POT 20.00K OHM 3/4W
102-000307-	00	POT 100.00K OHM 3/4W
102-000308-	00	NET RES NTWK 300145-6K-6K
102-000309-	00	POT 1.00M OHM 1/2W 20%
102-000310-	00	RES 20.00K OHM 2W 5%
102-000311-	00	RES 51.00 OHM 1/2W 5% PIHER
102-000312-	00	RES 7.32K OHM 1/4W 1%
102-000313-	00	RES 100.00 OHM 3W 5%
102-000314-	00	RES 125.00 OHM 3W 5%
102-000315-	00	RES 330.00 OHM 1/2W 2%
102-000316-	00	RES 6.8K OHM 1/2W 5%
102-000317-	00	RES 110.00 OHM 3W 5%
102-000318-	00	RES 14.70 OHM 1/8W 1%
102-000320-	00	RES 68.00 OHM 1/2W 5%
102-000321-	00	RES 3.01K OHM 1/8W 1%
102-000322-	00	RES 511.00 OHM 1/4W 1%
102-000323-	00	RES 1.47K OHM 1/8W 1%
102-000324-	00	RES 1.96K OHM 1/4W 1% METFILM
102-000325-	00	RES 3.24K OHM 1/4W 1% METFILM
102-000326-	00	RES 4.42K OHM 1/4W 1% METFILM
102-000327-	00	RES 4.99K OHM 1/4W 1% METFILM
102-000328-	00	RES 2222.00 OHM 1/10W .02%
102-000329-	00	RES 1778.00 OHM 1/10W .02%
102-000330-	00	RES 2667.00 OHM 1/10W .02%
102-000331-	00	RES 3333.00 OHM 1/10W .02%
102-000332-	00	RES 10.00K OHM 1/10W .02%
102-000333-	00	VRIS HV SURGE SUPPR
102-000334-	00	RES 30.00 OHM 3W 5%
102-000335-	00	RES 30.00 OHM 1W 5%
102-000336-	00	RES 1.00 OHM 25W 5%
102-000337-	00	RES 8.00 OHM 4W 1%
102-000338-	00	RES 30.00 OHM 10W 5%
102-000339-	00	RES 14.00 OHM 10W 1%
102-000340-	00	RES .10 OHM 5W 5%
102-000341-	00	RES 5.00K OHM 5W 1%
102-000342-	00	RES 510.00 OHM 2W 5%
102-000343-	00	RES 1.05K OHM 1/4W 1%
102-000344-	00	RES 1.21K OHM 1/4W 1%
102-000345-	00	RES 4.02K OHM 1/4W 1%
102-000346-	00	RES 2.05K OHM 1/4W 1%
102-000347-	00	RES 5.11K OHM 1/4W 1%
102-000348-	00	RES 1.00 OHM 30W 5%
102-000349-	00	RES 10.00 OHM 30W 5%
102-000351-	00	RES 14.00 OHM 10W 5%

PART NUMBER	REV	DESCRIPTION
102-000352-	00	RES 8.00 OHM 5W 1%
102-000353-	00	RES 33.00 OHM 10W 5%
102-000355-	00	RES 330.00 OHM 1/8W 1%
102-000356-	00	RES 140.00 OHM 1/8W 1%
102-000357-	00	RES 10.00 OHM 5W 5%
102-000358-	00	POT 20.00K OHM 1/2W 20%
102-000359-	02	NET 4-105+-2% 1/10W
102-000360-	00	RES 20.00K OHM 5W 5%
102-000361-	00	RES 10.00K OHM 5W 5%
102-000362-	00	RES 11.100 OHM 4W 5%
102-000363-	00	P.O.T. 500.00 OHM 1/4W 10%
102-000364-	00	RES 12.00 OHM 4W 5% NON-IND
102-000365-	00	RES 15.00 OHM 3W 5%
102-000366-	00	VRIS 1KV2610A10QS
102-000367-	00	RES 180.00 OHM 1/2W 5%
102-000368-	00	RES 110.00 OHM 5W 5%
102-000369-	00	RES 2.37K OHM 1/4W 1%
102-000370-	00	THM 230.00 OHM .006W 5% KB22L2
102-000371-	00	RES 196.00 OHM 1/8W 1%
102-000372-	00	RES 464.00 OHM 1/8W 1%
102-000373-	00	RES 300.00 OHM 1W 5%
102-000374-	00	RES 51.10K OHM 1/4W 1%
102-000375-	00	POT 200.00 OHM 1W 10%
102-000376-	00	RES 150.00 OHM 1W 5%
102-000377-	00	RES 3.00 OHM 2.5W 5% ELZH N
102-000378-	00	POT 100.00 OHM 3/4 10% CERMET
102-000380-	00	RES 931.00 OHM 1/4W 1%
102-000381-	00	RES 475.00 OHM 1/4W 1%
102-000382-	00	RES 442.00 OHM 1/4W 1%
102-000383-	00	RES 316.00 OHM 1/4W 1%
102-000384-	00	RES 150.00 OHM 1/4W 1%
102-000385-	00	RES 118.00 OHM 1/4W 1%
102-000386-	00	RES 100.00 OHM 1/2W 5%
102-000387-	00	RES 1.00 OHM 10W 5%
102-000388-	00	RES 1.00K OHM 1W 5%
102-000389-	00	RES 330.00 OHM 1/2W 5%
102-000390-	00	RES .10 OHM 2 1/2W 3%
102-000391-	00	RES 82.00 OHM 3W 1%
102-000392-	00	RES 680.00 OHM 1W 5% COMP
102-000393-	00	RES .20 OHM 1W 5%
102-000394-	00	POT 100.00 OHM 25T SQ 10% CERMET
102-000395-	00	RES 110.00 OHM 1/2W 5%
102-000396-	00	RES 5.00 OHM 225W OHMITE ADJ
102-000397-	00	RES 33.00K OHM 1/2W 5%
102-000398-	00	RES 30.10 OHM 1/8W 1%
102-000399-	00	RES 510.00 OHM 2W 5% WR WND
102-000400-	00	RES 5.00 OHM 25W +5%
102-000401-	00	RES 2.00 OHM 25W +5%
102-000402-	00	POT 4.0000 OHM 3W 10%
102-000403-	00	RES 13.50K OHM 1/4W 1%
102-000404-	00	POT 5.00K OHM
102-000405-	00	POT 20.00K OHM
102-000406-	00	POT 500.00 OHM
102-000407-	00	POT 1.00K OHM
102-000408-	00	POT 5.00K OHM
102-000409-	00	POT 10.00K OHM
102-000410-	00	POT 20.00K OHM
102-000411-	00	POT 50.00 OHM
102-000412-	00	RES 4.00 OHM 10W
102-000413-	00	RES .20 OHM 2W
102-000414-	00	RES 2.2K OHM 1/2W 0% W/W
102-000415-	00	RES HAMMER DRIVER 2310 800210-001
102-000416-	00	RES 34.00 OHM 1/4W +5%
102-000417-	00	RES 50.000 OHM 100W TR-AN500D
102-000418-	00	RES 15.00 OHM 25W TRAI150D
102-000419-	00	RES 1.10 OHM 1/2W +5%
102-000420-	00	RES 22.00 OHM 1/2W +5%
102-000421-	00	RES 10.00 OHM 10W +5% WW
102-000422-	00	RES RWR .30 OHM 7W +1%
102-000423-	00	RES 220.00 OHM 1W 570
102-000424-	00	RES 10.00 OHM 10W 10057-10
102-000425-	00	POT 1.00K OHM 1/2W 20%
102-000426-	00	POT 2.00K OHM 1/2W 20%
102-000427-	00	RES 2.00K OHM 1/2W 5%
102-000428-	00	RES 75.00 OHM 5W 5%
102-000429-	00	POT 500.00 OHM 1/2W %
102-000430-	00	POT 2.00K OHM 1/2W %
102-000431-	00	POT 10.00K OHM 1/2W %
102-000432-	00	RES 18.20K OHM 1/10W 1%
102-000433-	00	RES 47.50K OHM 1/10W 1%
102-000434-	00	RES 121.00K OHM 1/10W 1%
102-000435-	00	RES 332.00 OHM 1/4W 1%
102-000436-	00	RES 8.25K OHM 1/10W+1-1%
102-000437-	00	RES 2.00K OHM 1/2W-5+5%
102-000438-	00	RES 150.00 OHM 1/2W5+5%
102-000439-	00	RES 75.00 OHM 1/100-1+1%

PART NUMBER	REV	DESCRIPTION
102-000440-	00	RES 750.00 OHM 1/10W+1-1%
102-000441-	00	JUMPER INSULATED .625
102-000442-		VARIAC 20AMP 0-280V 3100-5120
102-000443-		POT 100.00 OHM 2W 5%
102-000444-		RES .40 OHM 20W 5%
102-000445-		POT 100.00 OHM 5W 10%
102-000446-		RES 97.24 OHM 25W 1%
102-000447-		REG 19.22 OHM 25W 1%
102-000448-		RES 24.00 OHM 25W 1%
102-000449-		RES 10.00 OHM 25W 1%
102-000450-		RES 12.00 OHM 25W 1%
102-000451-	00	SHUNT 100A +1-1% 6713
102-000452-		POT 50.00 OHM 100W 10%
102-000453-		POT 500.00 OHM 2W 10%
102-000454-	00	RES 38.30 OHM 1/4W 1%
102-000455-	00	RES 51.10 OHM 1/4W 1%
102-000456-	00	RES 100.00 OHM 1/4W 1%
102-000457-	00	RES 118.00 OHM 1/4W 1%
102-000458-	00	RES 121.00 OHM 1/4W 1%
102-000459-	00	RES 261.00 OHM 1/4W 1%
102-000460-	00	RES 301.00 OHM 1/4W 1%
102-000461-	00	RES 316.00 OHM 1/4W 1%
102-000462-	00	RES 562.00 OHM 1/4W 1%
102-000463-	00	RES 619.00 OHM 1/4W 1%
102-000464-	00	RES 825.00 OHM 1/4W 1%
102-000465-	00	RES 931.00 OHM 1/4W 1%
102-000466-	00	RES 1.40K OHM 1/4W 1%
102-000467-	00	RES 2.21K OHM 1/4W 1%
102-000468-	00	RES 9.11K OHM 1/4W 1%
102-000469-	00	RES 13.30K OHM 1/4W 1%
102-000470-	00	RES 200.00K OHM 1/4W 1%
102-000471-		RES 15.00 OHM 2W 1%
102-000472-		RES 5.00 OHM 5N 5%
102-000473-		RES 2.00 OHM 5N 5%
102-000474-		RES 5.00 50W 5%
102-000475-		RES 5.00 OHM 2KN 5%
102-000476-		RES 1.00 OHM 2KN 5%
102-000477-		RES 10.00 OHM 25W 5%
102-000478-		RES 20.00 OHM 5/N 10%
102-000479-	00	RES 75.00 OHM 1/2W 5%
102-000480-	00	RES 22.005 OHM 1/2W 5% CBN CMR
102-000481-	00	POT 50.00K OHM 1/2W 10%
102-000482-	00	RES 4.00 OHM 3W 5%
102-000483-	00	RES 1.00K OHM 3W 5% WW
102-000484-	00	RES 2.20K OHM 1W 5% CARBON
102-000485-	00	RES 1.50K OHM 1W 5% CARBON
102-000486-	00	RES 5.10K OHM 1W 5% CARBON
102-000487-	00	RES 0.50 OHM 5W 5% WW
102-000488-	00	RES 47.00 OHM 1W 5%
102-000489-	00	RES 2.20K OHM 1/2W 5%
102-000490-	00	RES 1.30 OHM 1/2W 5%
102-000491-	00	RES 5.60K OHM 1/2W 5%
102-000492-	00	RES 5.00 OHM 55W 5% FLAT
102-000493-	00	RES 0.50 OHM 55W 5% FLAT
102-000494-	00	RES 300.00 OHM 1/2W 5% CARBON
102-000495-	00	RES 1200.00 OHM 1W 5% WW
102-000496-	00	RES 620.00 OHM 1/2W 5% CARBON
102-000497-	00	RES 750.00 OHM 2W 20%
102-000498-		RES 0.40 OHM 20W 5%

PART NUMBER	REV	DESCRIPTION
103-000001-	00	CAP .01MF +80-20% 50V CER
103-000002-	00	CAP 6.8000MF +10-10% 35V TANT
103-000003-	00	CAP .2200MF +10-10% 20V TANT
103-000004-	00	CAP 470.0000PF +5-5% 500V MICA
103-000005-	00	CAP 820.0000PF +5-5% 300V MICA
103-000006-	00	CAP 220.0000PF +5-5% 500V MICA
103-000007-	00	CAP 50.0000MF +5-5% 50V TANT
103-000008-	00	CAP 6000.0000MF
103-000009-	00	CAP 220.0000PF
103-000010-	00	CAP 100.0000PF
103-000011-	00	CAP .2200MF
103-000012-	00	CAP .1000MF +5-5% 250V IL
103-000013-	00	CAP .5000MF
103-000014-	00	CAP 5.6000MF
103-000015-	00	CAP .0022MF -5+5% 500V
103-000016-	00	CAP 1.0000MF +10-10% 35V TANT
103-000017-	00	CAP 6.8000MF
103-000018-	00	CAP 6.8000MF +10-10% 6V TANT
103-000019-	00	CAP 25000.0000MF
103-000020-	00	CAP 48000.0000MF
103-000021-	00	CAP 25000.0000MF
103-000022-	00	CAP 13000.0000MF
103-000023-	00	CAP 530.0000MF
103-000024-	00	CAP 1000.0000MF
103-000025-	00	CAP 32000.0000MF
103-000026-	00	CAP 21000.0000MF +20-20% 40V E;
103-000026-	00	CAP 21000.0000MF +20-20% 40V ELEC
103-000027-	00	CAP 6000.0000MF +20-20% 10V ELEC
103-000028-	00	CAP 1000.0000MF
103-000029-	00	CAP 1100.0000MF
103-000030-	00	CAP 6.8000MF
103-000031-	00	CAP 100.0000PF +5-5% 500V MICA
103-000032-	00	CAP
103-000033-	00	CAP
103-000034-	00	CAP 122.0000PF
103-000035-	00	CAP 1200.0000PF +5-5% 100V MICA
103-000036-	00	CAP 8.0000MF +20-20% 50V TANT
103-000037-	00	CAP 47,0000MF +20-20% 20V TANT
103-000038-	00	CAP
103-000039-	00	CAP .0500MF +20-20% 12V CER
103-000040-	00	CAP 33.0000PF +5-5% 500V MICA
103-000041-	00	CAP 560.0000PF +5-5% 300V MICA
103-000042-	00	CAP 300.0000PF
103-000043-	00	CAP 21000.0000MF +20-20% 25V ELEC
103-000044-	00	CAP 12.0000PF +5-5% 500V MICA
103-000045-	00	CAP 2.2000MF +20-20% 20V TANT
103-000046-	00	CAP 330.0000PF +5-5% 100V MICA
103-000047-	00	CAP .0068MF +10-10% 100V RCAP
103-000048-	00	CAP 24000.0000MF +20-20% 40V ELEC
103-000049-	00	CAP 38000.0000MF +20-20% 20V ELEC
103-000050-	00	CAP 63000.0000MF
103-000051-	00	CAP 20000.0000MF +20-20% 10V ELEC
103-000052-	00	CAP 47.0000MF +20-20% 6V TANT
103-000053-	00	CAP 68.0000PF +5-5% 500V MICA
103-000054-	00	CAP .0100MF +10-10% 50V RCAP
103-000055-	00	CAP 100.0000PF +5-5% 100V RCAP
103-000056-	00	CAP 82.0000PF +5-5% 500V MICA
103-000057-	00	CAP 6.8000MF +50-20% 6.3V T/T
103-000058-	00	CAP
103-000059-	00	CAP 110.0000MF 40V
103-000060-	00	CAP 31000.0000MF +20-20% 40V ELEC
103-000061-	00	CAP 20000.0000MF +20-20% 20V ELEC
103-000062-	00	CAP 6.8000MF +50-20% 35V T/T
103-000063-	00	CAP 161-193MF 110V 60HZ
103-000064-	00	CAP FILTER MURATA SFB455D
103-000065-	00	CAP 1.0000MF +10-10% 35V T/T
103-000066-	00	CAP 6300.0000 % 20V ELEC
103-000067-	00	CAP 33000.0000 % 50V ELEC
103-000068-	00	CAP 47.0000MF +50-20% 6.3V T/T
103-000069-	00	CAP 1.5000MF +20-20% 35V ELEC
103-000070-	00	CAP .0220MF +10-10% 100V RCAP
103-000071-	00	CAP 27.0000PF +5-5% 500V MICA
103-000072-	00	CAP 150.0000PF +5-5% 500V MICA
103-000073-	00	CAP .1000MF +5-5% 50V MYLAR
103-000074-	00	CAP 100.0000MF % 15V TANT
103-000075-	00	CAP 4.7000MF +50-20% 50V TAG
103-000076-	00	CAP 7000.0000MF % 20V ELEC
103-000077-	00	CAP .1000MF +10-10% 200V TANT
103-000078-	00	CAP 130-156MF 110V 60HZ
103-000079-	00	CAP 5600.0000PF +10-10% 200V
103-000080-	00	CAP 47-56MF 200V 7
103-000080-	00	CAP 47-56MF 200V 60HZ
103-000081-	00	CAP 1200.0000MF % 40V ELEC
103-000082-	00	CAP 1200.0000MF % 20V ELEC
103-000083-	00	CAP 20000.0000MF 10V ELEC
103-000084-	00	CAP 22.0000MF 10V TAG
103-000085-	00	CAP .2200MF 100V MYLAR
103-000086-	00	CAP .1000MF 50V
103-000087-	00	CAP .4700MF 50V
103-000088-	00	CAP 3600.0000MF 50V
103-000089-	00	CAP 800.0000MF 50V ELEC
103-000090-	00	CAP .2000FD +75-10% 10V
103-000091-	00	CAP 98000.0000MF +75-10% 20V
103-000092-	00	CAP 66000.0000MF +75-10% 20V
103-000093-	00	CAP NOT ASSIGNED
103-000094-	00	CAP .0010MF +10-10% 1000V
103-000095-	00	CAP .1000MF +10-10% 400V MYLAR
103-000096-	00	CAP 12000.0000MF +75-10% 20V SANG
103-000097-	00	CAP 12000.0000MF +75-10% 40V SANG
103-000098-	00	CAP 5.0000PF +5-5% 500V MICA
103-000099-	00	CAP 6.0000PF +5-5% 500V MICA
103-000100-	00	CAP 10.0000PF +5-5% 500V MICA
103-000101-	00	CAP 51.0000PF +5-5% 500V MICA
103-000102-	00	CAP 270.0000PF +5-5% 500V MICA
103-000103-	00	CAP .0150MF +10-10% 100V
103-000104-	00	CAP 77000.0000MF +75-10% 20V ELEC
103-000105-	00	CAP 71000MF/ 63000MF
103-000106-	00	CAP 13000.0000MF
103-000107-	00	CAP 13000.0000MF 40V
103-000108-	00	CAP 22.0000MF 16V TAG
103-000110-	00	CAP 77000.0000MF +75-10% 20V ELEC
103-000111-	00	CAP .2300FD +75-10% 20V ELEC
103-000112-	00	CAP .6300FD +75-10% 6V ELEC
103-000113-	00	CAP 15.0000PF +5-5% 500V MICA
103-000114-	00	CAP 1.0000MF T20-20% 50V TANT
103-000115-	00	CAP 4.0000MF +50-20% 660V 60HZ
103-000116-	00	CAP .0500MF +50-20% 25V DISC
103-000117-	00	CAP .1000MF 250V 60HZ
103-000118-	00	CAP .4000MF 660V
103-000119-	00	CAP AC LINE FILTER,RFI PWRLINE #20K6
103-000120-	00	CAP 160.0000PF +5-5% 500V MICA
103-000121-	00	CAP 12.5000MF +6-6% 370V
103-000122-	00	CAP .0470MF +10-10% 100V MYLAR
103-000123-	00	CAP .0033MF +10-10% 100V MYLAR
103-000124-	00	CAP 1.0000MF +10-10% 50V MYLAR
103-000125-	00	CAP 2.2000MF +50-20% 35V T/T
103-000126-	00	CAP .1500FD +75-10% 6V ELEC
103-000127-	00	CAP .0220 MF +10-10% 100V MYLAR
103-000128-	00	CAP .3300MF +10-10% 50V MYLAR
103-000129-	00	CAP 98000.0000MF +75-10% 20V ELEC
103-000130-	00	CAP 6.0000MF 660V OIL FILLED
103-000131-	00	CAP .01MF 400V
103-000132-	00	CAP 500MF 25V
103-000133-	00	CAP 10MF 660V
103-000134-	00	CAP 150,000 MF 6V
103-000135-	00	CAP 1600.0000PF +5-5% 500V MICA
103-000136-	00	CAP 1.0000MF 400V
103-000138-	00	CAP 24.0000PF +5% 300V MICA
103-000139-	00	CAP 1000UF 25WV CRAMER WHB1000-25
103-000140-	00	CAP 15MFD 200-365VACGE45F165
103-000141-	00	CAP 5MFD 366-410VAC GE 45F273
103-000142-	00	CAP 1.0000PF +5-5% 500V MICA
103-000143-	00	CAP 2.0000PF +5-5% 500V MICA
103-000144-	00	CAP 3.0000PF +5-5% 500V MICA
103-000145-	00	CAP 4.0000PF +5-5% 500V MICA
103-000146-	00	CAP 7.0000PF +5-5% 500V MICA
103-000147-	00	CAP 8.0000PF +5-5% 500V MICA
103-000148-	00	CAP 18.0000PF +5-5% 500V MICA
103-000149-	00	CAP 20.0000PF +5-5% 500V MICA
103-000150-	00	CAP 22.0000PF +5-5% MICA
103-000151-	00	CAP 24.0000PF +5-5% 500V MICA
103-000152-	00	CAP 30.0000PF +5-5% 500V MICA
103-000153-	00	CAP 36.0000PF +5-5% 500V MICA
103-000154-	00	CAP 39.0000PF +5-5% 500V MICA
103-000155-	00	CAP 43.0000PF +5-5% 500V MICA
103-000156-	00	CAP 47.0000PF +5-5% 500V MICA
103-000157-	00	CAP 62.0000PF +5-5% 500V MICA
103-000158-	00	CAP 75.0000PF +5-5% 500V MICA
103-000159-	00	CAP 91.0000PF +5-5% 500V MICA
103-000160-	00	CAP 110.0000PF +5-5% 500V MICA
103-000161-	00	CAP 120.0000PF +5-5% 500V MICA
103-000162-	00	CAP 130.0000PF +5-5% 500V MICA
103-000163-	00	CAP 180.0000PF +5-5% 500V MICA
103-000164-	00	CAP 200.0000PF +5-5% 500V MICA
103-000165-	00	CAP 240.0000PF +5-5% 500V MICA
103-000166-	00	CAP 300.0000PF +5-5% 500V MICA
103-000167-	00	CAP 360.0000PF +5-5% 500V MICA
103-000168-	00	CAP 390.0000PF +5-5% 500V MICA
103-000169-	00	CAP 430.0000PF +5-5% 500V MICA
103-000170-	00	CAP 510.0000PF +5-5% 500V MICA
103-000171-	00	CAP 620.0000PF +5-5% 500V MICA

PART NUMBER	REV	DESCRIPTION
103-000172-	00	CAP 680.0000PF +5-5% 500V MICA
103-000173-	00	CAP 750.0000PF +5-5% 500V MICA
103-000174-	00	CAP 910.0000PF +5-5% 500V MICA
103-000175-	00	CAP 1000.0000PF +5-5% 500V MICA
103-000176-	00	CAP 1100.0000PF +5-5% 500V MICA
103-000177-	00	CAP 1300.0000PF +5-5% 500V MICA
103-000178-	00	CAP 1500.0000PF +5-5% 500V MICA
103-000179-	00	CAP 1800.0000PF +5-5% 500V MICA
103-000180-	00	CAP 2000.0000PF +5-5% 500V MICA
103-000181-	00	CAP 2200.0000PF +5-5% 500V MICA
103-000182-	00	CAP 2400.0000PF +5-5% 500V MICA
103-000183-	00	CAP 2700.0000PF +5-5% 500V MICA
103-000184-	00	CAP 3000.0000PF +5-5% 500V MICA
103-000185-	00	CAP 3300.0000PF +5-5% 500V MICA
103-000186-	00	CAP 3600.0000PF +5-5% 500V MICA
103-000187-	00	CAP 3900.0000PF +5-5% 500V MICA
103-000188-	00	CAP 4300.0000PF +5-5% 500V MICA
103-000189-	00	CAP 4700.0000PF +5-5% 500V MICA
103-000190-	00	CAP 5100.0000PF +5-5% 500V MICA
103-000191-	00	CAP 5600.0000PF +5-5% 500V MICA
103-000192-	00	CAP 6200.0000PF +5-5% 500V MICA
103-000193-	00	CAP 6800.0000PF +5-5% 100V MICA
103-000194-	00	CAP 7500.0000PF +5-5% 100V MICA
103-000195-	00	CAP 8200.0000PF +5-5% 100V MICA
103-000196-	00	CAP .0010MF +10-10% 100V MYLAR
103-000197-	00	CAP .0012MF +10-10% 100V MYLAR
103-000198-	00	CAP .0015MF +10-10% 100V MYLAR
103-000199-	00	CAP .0018MF +10-10% 100V MYLAR
103-000200-	00	CAP .0022MF +10-10% 100V MYLAR
103-000201-	00	CAP .0027MF +10-10% 100V MYLAR
103-000202-	00	CAP .0039MF +10-10% 100V MYLAR
103-000203-	00	CAP .0047MF +10-10% 100V MYLAR
103-000204-	00	CAP .0050MF +10-10% 100V MYLAR
103-000205-	00	CAP .0056MF +10-10% 100V MYLAR
103-000206-	00	CAP .0068MF +10-10% 100V MYLAR
103-000207-	00	CAP .0082MF +10-10% 100V MYLAR
103-000208-	00	CAP .0100MF +10-10% 100V MYLAR
103-000209-	00	CAP .0120MF +10-10% 100V MYLAR
103-000210-	00	CAP .0150MF +10-10% 100V MYLAR
103-000211-	00	CAP .0180MF +10-10% 100V MYLAR
103-000212-	00	CAP .0270MF +10-10% 100V MYLAR
103-000213-	00	CAP .0330MF +10-10% 100V MYLAR
103-000214-	00	CAP .0390MF +10-10% 100V MYLAR
103-000215-	00	CAP .0500MF +10-10% 100V MYLAR
103-000216-	00	CAP .0560MF +10-10% 100V MYLAR
103-000217-	00	CAP .0820MF +10-10% 100V MYLAR
103-000218-	00	CAP .1000MF +10-10% 100V MYLAR
103-000219-	00	CAP .1200MF +10-10% 100V MYLAR
103-000220-	00	CAP .1500MF +10-10% 100V MYLAR
103-000221-	00	CAP .1800MF +10-10% 100V MYLAR
103-000222-	00	CAP .2700MF +10-10% 100V MYLAR
103-000223-	00	CAP .3300MF +10-10% 100V MYLAR
103-000224-	00	CAP .4700MF +10-10% 100V MYLAR
103-000225-	00	CAP .5000MF +10-10% 100V MYLAR
103-000226-	00	CAP .5600MF +10-10% 100V MYLAR
103-000227-	00	CAP .6800MF +10-10% 100V MYLAR
103-000228-	00	CAP .8200MF +10-10% 100V MYLAR
103-000229-	00	CAP 1.0000MF +10-10% 100V MYLAR
103-000230-	00	CAP 1.2500MF +10-10% 100V MYLAR
103-000231-	00	CAP 1.5000MF +10-10% 100V MYLAR
103-000232-	00	CAP 2.0000MF +10-10% 100V MYLAR
103-000233-	00	CAP 3.0000MF +10-10% 100V MYLAR
103-000234-	00	CAP 4.0000MF +10-10% 100V MYLAR
103-000235-	00	CAP .0680MF +10-10% 100V MYLAR
103-000236-	00	CAP .3900MF +10-10% 100V MYLAR
103-000237-	00	CAP 50.0000PF +5-5% 500V MICA
103-000238-	00	CAP 2500.0000PF +5-5% 500V MICA
103-000239-	00	CAP 500.0000PF +5-5% 500V MICA
103-000240-	01	CAP LINE FILTER EMI-F-0441
103-000241-	00	CAP 27.0000PF +5-5% 300V MICA
103-000242-	00	CAP .1000MF +20-20% 200V FILM
103-000243-	00	CAP LINE FILTER RFI EMI-F-0458
103-000244-	00	CAP .1 MF 16V
103-000245-	00	CAP MOTOR START 101/A
103-000246-	00	CAP 88-108 UF UP
103-000247-	00	CAP 4600.0000MF
103-000248-	00	CAP 10.0000MF
103-000249-	00	CAP 17.5000MF
103-000250-	00	CAP 3.0000MF
103-000251-	00	CAP 4.0000MF
103-000252-	00	CAP .1000MF -20% 50V CER
103-000253-	00	CAP 6.8000MF +10% 6V T/T
103-000254-	00	CAP 3.000MFP 370V
103-000255-	00	CAP 9000.0000MF 40V
103-000256-	00	CAP 160.0000MF 25V
103-000257-	00	CAP 50.0000MF 100V TC-HH506E
103-000258-	00	CAP 25090000MF 16V TC-WA257
103-000259-	00	CAP 6.0000MF 660V NOM (GE45F608)
103-000260-	00	CAP 1600.0000MF 10074-16
103-000261-	00	CAP 4.0000MF 6% 660V
103-000262-	00	CAP 100.0000PF +5-5% 50V CER
103-000263-	00	CAP .0470MF +20-20% 50V CER
103-000264-	00	CAP 1.0000MF -0+100% 50V CE/RDL
103-000265-	00	CAP 27.0000PF +5-5% 50V CER
103-000266-	00	CAP 180.0000PF +5-5% 50V CER
103-000267-	00	CAP 220.0000PF +5-5% 50V CER
103-000268-	00	CAP 360.0000PF +5-5% 50V CER
103-000269-	00	CAP 470.0000PF +5-5% 50V CER
103-000270-	00	CAP 820.0000PF +5-5% 50V CER
103-000271-	00	CAP 1200.0000PF +10-10% 50V CER
103-000272-	00	CAP 5600.0000PF +10-10% 50V CER
103-000273-	00	CAP 6800.0000PF +10-10% 50V CER
103-000274-	00	CAP .010MF +8-20% 50V CER
103-000275-	00	CAP .0100MF +10-10% 50V CER
103-000276-	00	CAP .015MF +10-10% 50V CER
103-000277-	00	CAP .022MF +10-10% 50V CER
103-000278-	00	CAP 2.2000MF -0+100% 50V CE/AXL
103-000279-	00	CAP 2.2000MF +80-20% 50V CER
103-000280-	00	CAP 2.2000MF -0+100% 50V CE/RDL
103-000281-	00	CAP .0470MF +80-20% 50V CER
103-000282-	00	CAP 150.0000PF +5-5% 50V CER
103-000283-	00	CAP 13800.0000MF 15VDCW
103-000284-	00	CAP 3.0000MF 10%
103-000285-	00	CAP 6200.0000MF 75VDCW
103-000286-	00	CAP .2200MF +20-20% 100V CER-R
103-000287-	00	CAP 100.0000MF +20-20% 25V ELEC
103-000288-	00	CAP LINE FILTER EMI PWR 10R6 10A
103-000289-	00	CAP .0050MF +20-20 500V CER
103-000290-	00	CAP 1.0000MF -0+100% 50V CE/AXL
102-000291-		CAP 24000.0000MF +20-20% 75V
103-000292-		CAP 38000.0000MF +10-10% 40V
103-000293-	00	CAP 3300.0000MF +80-20% 100V
103-000294-	00	CAP 20.0000MF -10+75% 100V
103-000295-	00	CAP 5600.0000PF +10-10% 50V CR
103-000296-	00	CAP 9000.0000MF +100-10% 50V ELECT
103-000297-	00	CAP 1500.0000PF +20-20% 50V CER
103-000298-	00	CAP 330.0000PF +5-5% 50V CER
103-000299-	00	CAP 160.0000PF +5-5% 50V CER
103-000300-	00	CAP 68.0000PF +5-5% 50V CER
103-000301-	00	CAP 33.0000PF +5-5% 50V CER
103-000302-	00	CAP 20.0000PF +5-5% 50V CER
103-000303-	00	CAP 15.0000PF +5-5% 50V CER
103-000304-	00	CAP 10.0000PF +5-5% 50V CER
103-000305-	00	CAP 5.0000PF +5-5% 50V CER
103-000306-	00	CAP 4.0000PF +5-5% 50V CER
103-000307-	00	CAP 2.0000PF +5-5% 50V CER
103-000308-	00	CAP 470.0000PF +1-1% 50V CER
103-000309-		CAP EMI DC BUTTON FILTER 1021-000
103-000310-		CAP 0.0022MF +10-10% 50V CER

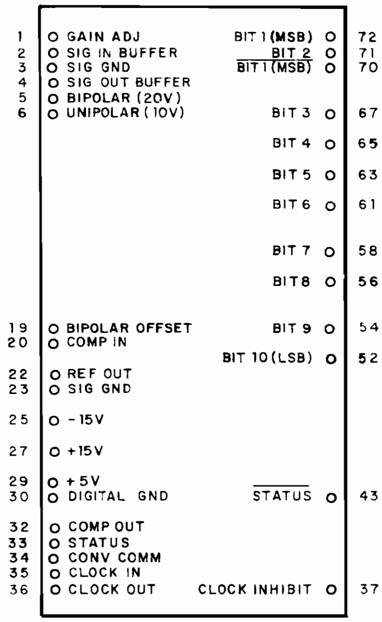
PART NUMBER	REV	DESCRIPTION
104-000001-	00	XFMR BALON NOVA
104-000002-	00	XFMR 3:1
104-000003-	00	XFMR 1:1
104-000004-	00	XFMR F-109U
104-000005-	05	XFMR F-60U
104-000006-	00	XFMR CHOKE CLOCK S/N
104-000007-	00	XFMR
104-000008-	00	XFMR
104-000009-	00	XFMR
104-000010-	03	XFMR PWR-S/N
104-000011-	00	XFMR
104-000012-	01	XFMR MEMORY
104-000013-	00	XFMR BALON S/N
104-000014-	00	XFMR F-106Z
104-000015-	00	XFMR N16
104-000016-	00	XFMR ISOLATION 230/115
104-000017-	03	XFMR PWR 1200/800
104-000018-	00	XFMR CHOKE 100MH +5-5%
104-000019-	00	XFMR SOLENOID
104-000022-	04	XFMR PWR - 1210
104-000023-	02	XFMR PWR - 1220/820
104-000026-	00	XFMR F-108U 115V-24V 96VA
104-000028-	01	XFMR CENTER TAP BIFILAR COIL
104-000029-	00	XFMR SINGLE WOUND COIL
104-000030-	00	XFMR STEP DOWN/P5555
104-000031-	00	XFMR STEP DOWN 230/115 50/60HZ VA1000
104-000032-	00	XFMR 15 MH COIL
104-000033-	00	XFMR 1 MH COIL
104-000034-		XFMR COIL ASSY +- 15 MHD
104-000035-		XFMR COIL ASSY +5 MHD
104-000036-	00	COIL HOLD ELECTROMAGNET 4000 TURNS
104-000037-	00	XFMR TRIAD F107Z
104-000038-	01	XFMR MMC - 4814
104-000039-	00	XFORMER 5-28/15-10
104-000040-	00	XFMR CONSTANT VOLTAGES 5-35/15-10
104-000041-	01	XFMR PWR LINEAR 170W
104-000042-		XFMR CONSTANT VOLTAGE
104-000043-	03	XFMR 36 VOLT 16 AMP & 36 VOLT 13 AMP
104-000044-	00	XFMR 50HZ CUT 600VA
104-000045-	00	XFMR CUT 5-60/15-15 60HZ
104-000046-	00	XFMR CVT 5-60/15-15 50HZ
104-000047-	02	XFMR COIL
104-000048-	00	XFMR 24:8
104-000049-	00	XFMR 110/220V 50HZ
104-000050-	00	XFMR PULSE, BH ELECTRONICS
104-000051-	01	XFMR 115V TO 230V, STEP UP, 1000VA
104-000052-	00	XFMR MMC 5030 1:12
104-000053-	00	COIL CLOCK HEAD 35 TURNS
104-000054-	00	XFMR 25.2V CT @ .060A MICROTRAN 2512
104-000055-	00	INDTR .10 MH + 10-10%
104-000056-	00	INDTR .12 MH +10-10%
104-000057-	00	INDTR .15 MH +10-10%
104-000058-	00	INDTR .18 MH +10-10%
104-000059-	00	INDTR .22 MH +10-10%
104-000060-	00	INDTR .27 MH +10-10%
104-000061-	00	INDTR .33 MH +10-10%
104-000062-	00	INDTR .39 MH +10-10%
104-000063-	00	INDTR .47 MH +10-10%
104-000064-	00	INDTR .56 MH +10-10%
104-000065-	00	INDTR .68 MH +10-10%
104-000066-	00	INDTR .82 MH +10-10%
104-000067-	00	INDTR 1.20 MH +10-10%
104-000068-	00	INDTR 1.50 MH +10-10%
104-000069-	00	INDTR 1.80 MH +10-10%
104-000070-	00	INDTR 2.20 MH +10-10%
104-000071-	00	INDTR 2.70 MH +10-10%
104-000072-	00	INDTR 3.30 MH +10-10%
104-000073-	00	INDTR 3.90 MH +10-10%
104-000074-	00	INDTR 4.70 MH +10-10%
104-000075-	00	INDTR 5.60 MH +10-10%
104-000076-	00	INDTR 6.80 MH +10-10%
104-000077-	00	INDTR 8.20 MH +10-10%
104-000078-	00	INDTR 10.00 MH +10-10%
104-000079-	00	INDTR 12.00 MH +10-10%
104-000080-	00	INDTR 18.00 MH +10-10%
104-000081-	00	INDTR 22.00 MH +10-10%
104-000082-	00	INDTR 27.00 MH +5-5%
104-000083-	00	INDTR 33.00 MH +5-5%
104-000084-	00	INDTR 39.00 MH +5-5%
104-000085-	00	INDTR 47.00 MH +5-5%
104-000086-	00	INDTR 56.00 MH +5-5%
104-000087-	00	INDTR 68.00 MH +5-5%
104-000088-	00	INDTR 82.00 MH +5-5%
104-000089-	00	INDTR 120.00 MH +5-5%
104-000090-	00	INDTR 150.00 MH +5-5%
104-000091-	00	INDTR 180.00 MH +5-5%
104-000092-	00	INDTR 220.00 MH +5-5%
104-000093-	00	INDTR 270.00 MH +5-5%
104-000094-	00	INDTR 330.00 MH +5-5%
104-000095-	00	INDTR 390.00 MH +5-5%
104-000096-	00	INDTR 470.00 MH +5-5%
104-000097-	00	INDTR 560.00 MH +5-5%
104-000098-	00	INDTR 680.00 MH +5-5%
104-000099-	00	INDTR 820.00 MH +5-5%
104-000100-	00	INDTR 1000.00 MH +5-5%
104-000101-	00	INDTR 1200.00 MH +10-10%
104-000102-	00	INDTR 1500.00 MH +10-10%
104-000103-	00	INDTR 1800.00 MH +10-10%
104-000104-	00	INDTR 2200.00 MH +10-10%
104-000105-	00	INDTR 2700.00 MH +10-10%
104-000106-	00	INDTR 3300.00 MH +10-10%
104-000107-	00	INDTR 3900.00 MH +10-10%
104-000108-	00	INDTR 4700.00 MH +10-10%
104-000109-	00	INDTR 5600.00 MH +10-10%
104-000110-	00	INDTR 6800.00 MH +10-10%
104-000111-	00	INDTR 8200.00 MH +10-10%
104-000112-	00	INDTR 10000.00 MH +10-10%
104-000113-	00	XFMR POWER MERRIMACK
104-000114-	00	XFMR ASSY 12-115V M600L 20015601
104-000115-	00	XFMR ASSY 24-115V M600L 20015501
104-000116-	00	XFMR 50/60HZ 115V M600L 00000134
104-000117-	00	INDTR 330.00 MH -10%
104-000118-	01	XFMR LINEAR PWR CRT 6012 MMC5189
104-000119-	00	XFMR POWER FOR 4080B BT383
104-000120-	00	XFMR CONSTANT VOLTAGE ELB7-7 60HZ
104-000121-	00	XFMR 50HZ 7SLOT CON VLTG
104-000122-	00	DL 0-50 NS DAVEN DL800
104-000123-		XFMR CON VLTG 16 SLOT 60HZ
104-000124-		XFMR CON VLTG 16 SLOT 50HZ
104-000125-	00	TRANSFORMER POWER DRIVE 50-55033-3
104-000126-	00	XFMR 4.54VA 50/60HZ PC2608
104-000128-	00	XFMR IC REGULAR 5V
104-000129-	00	XFMR TRANSFORMER ASSY
104-000130-	00	XFMR DELAY LINE 35NSEC
104-000131-		XFMR VARIAC W30463
104-000132-	00	XFMR COIL ASSY
104-000133-		XFMR CONSTANT VOLTAGE 60HZ
104-000134-	00	VARIAC 240W 50/60HZ 3150-5110
104-000135-	00	DELAY LINE 200OHM 75NSGC 5%TOL
104-000136-	00	XFMR PWR 50/60HZ 5379
104-000137-	00	INDTR 56MH #10% WEE-56,000
104-000138-	00	XFMR CONSTANT VOLTAGE MMC5537
104-000139-		XFMR PWR 5518

PART NUMBER	REV	DESCRIPTION
110-000040-	00	RELAY POTTER BRUMFIELD 6VAC PMT 17A
110-000041-	00	RELAY JRM 1000 PB 1AMP 10 WATT
110-000042-	00	RELAY 4897-990
110-000043-	01	RELUCTANCE PICK-UP 6815013
110-000044-	00	SWITCH THUMBWHEEL #189220 1 POLE DEC.
110-000045-	01	SWITCH 7103SY PWGEAV-2-X
110-000047-	00	RELAY 50HZ 230V
110-000048-	00	SWITCH 435166-1
110-000049-	00	SWITCH DIP 8 POS AMP 435166-5
110-000050-	00	SWITCH DIP 4 POS AMP 435166-3
110-000051-	00	SWITCH CK 73034ZQEJ2
110-000052-	00	AMP DISTRIBUTOR 4325166-3
110-000053-	00	SWITCH DIP 5 POS AMP 435166-3
110-000054-	00	RELAY DRY REED W103MPCX-4
110-000055-	00	RELAY DRY REED W101MPCX-3
110-000056-	00	RELAY MERC WETTED W131MPCX-4
110-000057-	00	RELAY MERC WETTED W132MPCX-4
110-000058-	00	SWITCH 7203ZQEJ2 C&K
110-000059-	00	SWITCH DP3P ROCKER
110-000060-	00	SOLENOID LEDEX #124911-030
110-000061-	00	SWITCH SPST CUTLER HAMMER 7561K74
110-000062-	00	RELAY W107DIP-1
110-000063-	00	SWITCH 8-POS AMP 435166-5
110-000064-	00	SWITCH 3PDT 15A/CONTACT
110-000065-	01	SWITCH MINI TOGGLE MOMENTARY
110-000066-	01	SWITCH MINI TOGGLE MAINTAINING
110-000067-	04	SWITCH SELECTOR
110-000068-	03	SWITCH SELECTOR (POWER)
110-000069-	01	SWITCH TOGGLE, MOMENTARY
110-000070-	01	SWITCH TOGGLE, MAINTAIN
110-000071-	00	SWITCH MICRO #311SM701-T
110-000072-	00	SW PRESS 10" FAIRCHILD #PSF100A-10C
110-000073-	00	SW PRESS 20" FAIRCHILD #PSF100A-20C
110-000074-	00	SWITCH MOM ACT 101 SN11
110-000075-	00	SWITCH OAK 390 DP TWO POS
110-000076-	00	SWITCH LOW TORQUE 1-NO, CHERRY #E51-51T
110-000077-	00	SWITCH .251 SIM RLR, MICRO #311SM4-T
110-000078-	00	SWITCH FLEX LEAF W/RLR, MICRO #111SM2-T
110-000079-	00	SWITCH OPT 2-CHAN, HEI #0S562A-060LW
110-000080-	00	RELAY TP DR 1435-IC-12D GUARDIAN
110-000081-	00	SWITCH ON/OFF 101/A 525492001
110-000082-	00	SWITCH SELECT 101/A 525493001
110-000083-	00	SWITCH TOP/FORM 101/A 525494001
110-000084-	00	SWITCH OVERRIDE 101/A 525495001
110-000085-	00	SWITCH LINIT (REED) 525721001
110-000086-	00	SWITCH & INDICATOR FORWARD 100104-001
110-000087-	00	SWITCH & INDICATOR LOAD 100104-002
110-000088-	00	SWITCH & INDICATOR ON LINE 100104-003
110-000089-	00	SWITCH & INDICATOR REVERSE 100104-004
110-000090-	00	SWITCH REWIND 100130-001
110-000091-	00	SWITCH RESET 100130-002
110-000092-	00	SWITCH MICRO 15MI-T/J55 100012
110-000093-	00	SWITCH PAPER OUT 525272001
110-000094-	00	SWITCH & INDICATOR POWER 100179-001
110-000095-	00	SWITCH LOAD RUN 10541
110-000096-	00	SWITCH TOGGLE UCC ASR 33 197081
110-000097-	00	RELAY UCC ASR 33 181810
110-000098-	00	RELAY AC 25A 120V M600L 00000901
110-000099-	00	SWITCH PB SPDT POWER 00000319
110-000100-	00	SWITCH PB SPDT RESET 00000320
110-000101-	00	SWITCH PB SPST STOP 00000321
110-000102-	00	RELAY TIME DELAY CDS 114 90380-001
110-000103-	00	RELAY GEN PURP CDS 114 90381-001
110-000104-	00	SWITCH MICRO CDS 114 90734-001
110-000105-	00	RELAY POWER DIST CDS 114 90382-001
110-000106-	00	SWITCH MICRO 2310 800129-001
110-000107-	00	SWITCH MERCURY 2310 800222-001
110-000108-	00	SWITCH 2310 800303-001
110-000109-	00	SWITCH MOMENTARY 2310 800305-001
110-000110-	00	SWITCH 2310 800306-001
110-000111-	00	SWITCH RIBBON REVERSE 206840-001
110-000112-	00	SWITCH PAPER OUT UPPER 212634-001
110-000113-	00	SWITCH PAPER OUT LOWER 214959-001
110-000114-	00	SWITCH MOM PUSH CHEAT INTLK E69-30A
110-000115-	00	RELAY DBL POLE, 10SEC DELAY
110-000116-	00	SWITCH TOGGLE 3 POSITION TDT02DD93
110-000117-	00	SWITCH REWIND 150006701
110-000118-	00	SWITCH C&K 52 PODL HNDL U33-J2 CRT DSP
110-000119-	00	SWITCH ALT ACTION 416004901
110-000120-	00	SWITCH MOM ACTION 416004902
110-000121-	00	RELAY 384105013
110-000122-	00	SWITCH PUSH 805015006
110-000123-	01	SWITCH MINI, TOGGLE
110-000124-	00	SWITCH PAPER OUT LWR 2440 218811-001
110-000125-	00	SWITCH PAPER OUT #1 2440 218086-001
110-000126-	00	SWITCH PAPER OUT #1 2240 800944-001
110-000127-	00	SWITCH ROCKER 2440 800931-001
110-000128-	00	SWITCH PAPER OUT LWR 2230 235595-001
110-000129-	00	SWITCH LIMIT SW ASSY 2230 233585-001
110-000130-	00	SWITCH TOGGLE 2230 800502-001
110-000131-	00	SWITCH TOGGLE 2230 800502-003
110-000132-	00	SWITCH MINI TOGGLE
110-000133-	00	SWITCH SNAP-ACTION 100252-001
110-000134-	00	SWITCH SUMP PUMP F59A-2
110-000135-	00	SWITCH PUSH TYPE 416004903
110-000136-	00	SWITCH REWIND 150006701
110-000137-	00	SWITCH ARROW-HART DPST #82607
110-000138-	00	SWITCH HOUSING
110-000139-	00	SWITCH SNAP ACTION SPDT 120-563
110-000140-	00	SWITCH AUTO SHUT 120-851
110-000141-	00	SWITCH DOOR INTERLOCK 120-865
110-000142-	00	SWITCH PUSHBUTTON 120-965
110-000143-	00	RELAY DPST. R40-E2-W2-V200
110-000144-	00	RELAY SOCKET W/RTNR R40-S410 R40-P33
110-000145-	00	SWITCH HOPPER ACTUATOR 20111301
110-000146-	00	SWITCH HOPPER EMPTY ASSY 20137601
110-000147-	00	SWITCH OPTICAL SW ASSY 20127601
110-000148-	00	SWITCH TACTILE (STOP START)
110-000149-	00	SWITCH 2 POLE (POWER) 00000947
110-000150-	00	SWITCH REED 01045-001
110-000151-	00	SWITCH ROTARY 9 POS 2 POL 01017-003
110-000152-	00	SWITCH SLIDE SPOT 01017-004
110-000153-	00	SWITCH SLIDE 2 POL 2 POS 01017-005
110-000154-	00	SWITCH 3P PROTECTOR 60HZ 250V A/RPAX
110-000155-	00	SWITCH THUMBWHEEL EECO 8012G
110-000156-	00	RELAY 12 VOLT 801010-001
110-000157-	00	RELAY REED 50VA CONTACTS 6VDC COIL
110-000158-	00	SWITCH WRITE ENABLE ASSY 200378
110-000159-	00	SWITCH MAC-100-1 MUG HD CTG DISK
110-000160-	00	RELAY BREAK 100215
110-000161-		SWITCH BSIC V3L-1420D8 CTG DISK
110-000162-	00	SWITCH POWER 120-976
110-000163-	00	SWITCH CARTRIDGE INTERLOCK 15250
110-000164-	00	RELAY 6PDT 6-3V W67CSX-11
110-000165-	00	SWITCH SPDT PUSH ON-OFF MSP1050
110-000166-		SWITCH 15120
110-000167-		SWITCH 1405
110-000168-		SWITCH JBT MS25068-23
110-000169-		SWITCH C&H 7561K74-F27
110-000170-		SWITCH ROTARY 2501
110-000171-		SWITCH 5 POS 6P JV9007
110-000172-		SWITCH ROTARY 1403
110-000173-		SWITCH ROTARY CTS T205 12 POS
110-000174-		SWITCH ROTARY CTS T2053 POS
110-000175-		RELAY 15A CONT 6W 250HM W88KX-1
110-000176-	00	SWITCH PACK DETECT AA01AA
110-000177-		SWITCH ROTARY JV9001 1P 2-17
110-000178-	00	SWITCH C+K 5A UL APR DPDT U213ZQJX
110-000179-	00	SWITCH MINI TOGGLE MNTN DPOT
110-000180-	00	SWITCH CLEAR/DETECT 44 15300
110-000181-	00	SWITCH WRITE PROTECT 70682
110-000182-	00	SWITCH LOAD/RUN 44 10709
110-000183-	00	RELAY REED 3VA FORM C W172DIP-4
110-000184-		SWITCH 3P PROT 230/50
110-000185-		SWITCH 6 POS ROTARY CTS T-226
110-000186-	00	SWITCH DPDT 3 POSITION
110-000187-	00	SWITCH INDICATING PLATE MAN/AUTO
110-000188-	00	SWITCH LOCKING RING FOR 3 POS SW
110-000189-	00	SWITCH DUAL IN-LINE 435385-4 AMP
110-000190-	00	SWITCH DBL POLE SGL THROW CARLING
110-000191-	00	RELAY SOLID STATE 240V 10AMP
110-000192-	00	SWITCH OPTICAL OS-561A-060W

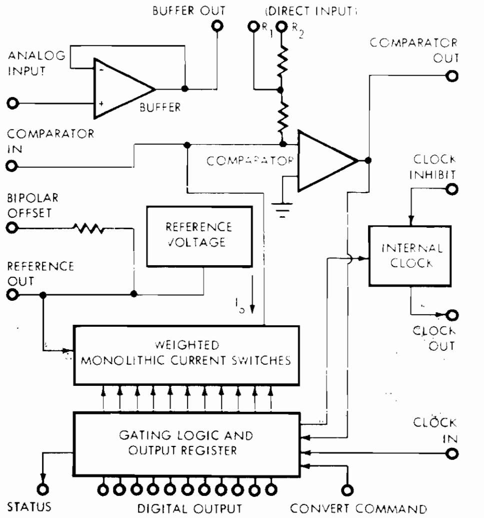
116000007

A/D Converter

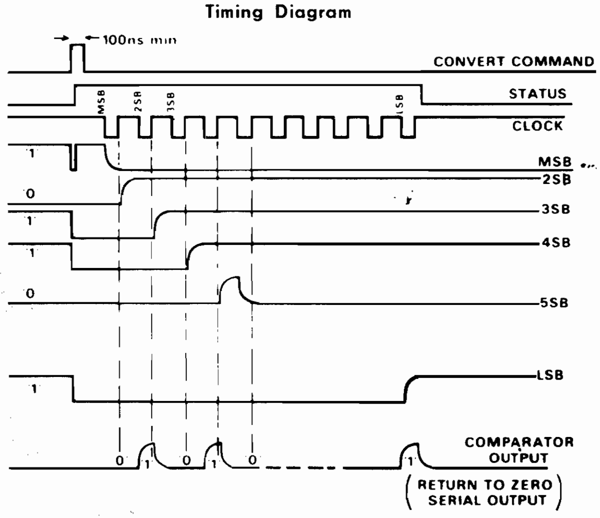
Pin Configuration
Top View



Block Diagram



Timing Diagram



Pin Designations

Pin No.		Pin No.	
1	Gain Adj.	72	Bit 1 (MSB)
2	Sig. In Buffer	71	Bit 2
3	Sig. Grd	70	Bit 1 (MSB)
4	Sig. Out Buffer	69	No pin
5	Bipolar (20V)	68	No pin
6	Unipolar (10V)	67	Bit 3
7	No pin	66	No pin
8	No pin	65	Bit 4
9	No pin	64	No pin
10	No pin	63	Bit 5
11	No pin	62	No pin
12	No pin	61	Bit 6
13	No pin	60	No pin
14	No pin	59	No pin
15	No pin	58	Bit 7
16	No pin	57	No pin
17	No pin	56	Bit 8
18	No pin	55	No pin
19	Bipolar Offset	54	Bit 9
20	Comp. In	53	No pin
21	No pin	52	Bit 10 (LSB)
22	Ref. Out	51	No pin
23	Sig. Grd	50	No pin connection
24	No pin	49	No pin
25	-15V	48	No pin connection
26	No pin	47	No pin
27	+15V	46	No pin
28	No pin	45	No pin
29	+5V	44	No pin
30	Digital Grd	43	STATUS
31	No pin	42	No pin
32	Comp. Out	41	No pin
33	Status	40	No pin
34	Conv. Comm.	39	No pin
35	Clock In	38	No pin
36	Clock Out	37	Clock Inhibit

The 116000007 circuit module is a 10-bit binary analog-to-digital converter capable of $\pm 1/2$LSB.

PART NUMBER	REV	DESCRIPTION
111-000000-	00	DEVICE CONN CARD READER
111-000001-	00	CONN 9 CONTACT PLUG DEC 9P WITH PINS
111-000002-	00	CONN 9 CONT SKT DEC 9S SZ 20 WITH PNS
111-000003-	00	CONN 25P ITT DBC25FO (DBC25P)
111-000004-	00	CONN 25 CONT SKT DBC 25S SZ 20 W/PNS
111-000005-	00	CONN 50 CONT PLUG DDC 50P SZ 20 W/PNS
111-000006-	00	CONN 50 CONT SKT DDC 50S SZ 20 W/PNS
111-000007-	00	CONN 19 CONT PLUG 20E19P WITH PINS
111-000008-	00	CONN 19 CONT SKT 2DE19S WITH PINS
111-000009-	00	CONN 52 CONT PLUG 2DB52P WITH PINS
111-000010-	00	CONN 52 CONT SKT 2DB5ES WITH PINS
111-000011-	00	CONN 100 CONT PLUG 2DD100P WITH PINS
111-000012-	00	CONN 100 CONT SKT 2DD100S WITH PINS
111-000013-	00	CONN 20-18 CONTACT PIN 030-1954
111-000014-	00	CONN 20-18 CONTACT SOCKET 030-1
111-000015-	00	CONN 20 CONTACT PIN 030-1952-00
111-000016-	00	CONN 20 CONTACT SOCKET 030-1953
111-000017-	00	CONN 22 CONTACT PIN 031-9540-00
111-000018-	00	CONN 22 CONTACT SOCKET 030-9542
111-000019-	00	CONN JUNCTION SHELL DE 24657
111-000020-	00	CONN JUNCTION SHELL DB24659
111-000021-	00	CONN JUNCTION SHELL DD24661
111-000022-	00	CONN SCREW LOCK ASSY FEMALE D204018-2
111-000023-	00	CONN SCREW LOCK MALE D20419-16
111-000024-	00	CONN SCREW LOCK MALE 20419-21
111-000025-	00	CONN SCREW LOCK MALE 20420-15
111-000026-	00	CONN A/C OUTLET PS 1369
111-000027-	00	CONN CABLE 20 DUAL POS AMP 86148-1
111-000028-	00	CONN PC HW-50D0-111
111-000029-	00	CONN CONTACT COMP LD 4-330808-9
111-000030-	00	CONN DIP SOCKET 16 PIN 041-001 112N
111-000031-	00	TERM POST 025SQ .287 AMP 86144-4
111-000032-	00	CONN FASTON RECEPTACLE SERIES 250
111-000033-	00	TERM RCPT 250 22-18 AWG AMP 42628-2
111-000034-	00	TERM RCPT 250 16-14 AWG AMP 42332-4
111-000035-	00	TERM R TNG #10 STUD 16-14AMP 2-31903-2
111-000036-	00	TERM R TNG #10 STUD 22-16AMP 2-31889-3
111-000037-	00	TERM R TNG #6 STUD 22-16 AMP 2-32403-1
111-000038-	00	TERM RCPT 187 22-18 AWG AMP 60972-3
111-000039-	00	TAB POLARIZING WINCHESTER 109-8340-1
111-000040-	00	CONN CABLE 22 DUAL POS AMP 86148-2
111-000041-	00	CONN RCPT 50 DUAL POSN AMP 86018-2
111-000042-	00	TERM TAB 250 .097 STUD 90AMP 41204
111-000043-	00	CONN 36 CONT FOR DISK
111-000044-	00	TERM TAB 250 .130 STUD 90 AMP 42117-2
111-000045-	00	TERM TAB 250 .130 STUD OFS AMP 42506-2
111-000046-	00	CONN T&B 18RA-6F
111-000047-	00	CONN WIRE SPLICE T & B 2RBR
111-000048-	00	TERM RCPT 187 20-16 FLG AMP 42486-2
111-000049-	00	CONN TERM AMP
111-000050-	00	CONN HI-CLAMP PPC-11
111-000051-	00	CONN FASTENER CB4-2 1/8 DIA BUTTON
111-000052-	00	CONN 6 PIN AM
111-000053-	00	CONN DISK FROM 111-000-043 LG
111-000054-	00	CONN DISK FROM 111-000-043 SM
111-000055-	00	CONN T&B RBB-25
111-000056-	00	CONN SPLICE 18-12AWG T&B RCC-26
111-000057-	00	TERM TAB 250 130 STUD 1PR AMP 41480
111-000058-	00	CONN AMP 85969-2 CRP 24-20 AWG
111-000059-	00	CONN AMP 1-480435-0
111-000060-	00	CONN CONTACT MALE D-110238-2
111-000061-	00	CONN SOCKET FEMALE D110238-3
111-000062-	00	CONN SOLDER SLEEVE D142-51
111-000063-	00	CONN HAYCO DC-201 BLACK
111-000064-	00	CONN HAYCO DC-201 AMBER ORANGE
111-000065-	00	CONN HAYCO T-101-S TIN PLATE TAB
111-000066-	00	CONN MAG TAPE 1800-22 MOLEX
111-000067-	00	CONN MAG TAPE MOLEX PINS 1799-T
111-000068-	00	CONN AMPHENOL 17-10500 MALE 50
111-000069-	00	CONN STYLE A 5353867
111-000070-	00	CONN STYLE B 5353868
111-000071-	00	CONN TERMINAL CONTACT 66341-2
111-000072-	00	CONN 6 CIRCUIT FASTON P/18 480003-5
111-000073-	00	CONN CONTACT PC 125CF 50
111-000074-	00	CONN CONTACT TERMINAL 60413-1
111-000075-	00	TERM POST 025SQ .210 AMP 86144-8
111-000076-	00	CONN TERMINAL BUSH GREEN DC 87-3-2
111-000077-	00	CONN TERMINAL BUSH ORG DC-87-3-2
111-000078-	00	CONN TERMINAL TAB BRASS T-202-55
111-000079-	00	CONN 26 POSITION 583679-1
111-000080-	00	CONN MOLEX 1490 RECEPTICAL
111-000081-	00	TERM FEM .093 14 TO 20 GA MOLEX 1189
111-000082-	00	CONN MOLEX 1490 PLUG
111-000083-	00	TERM MALE .093 14 TO 20 GA MOLEX 1190
111-000084-	00	CONN AMPHENOL MIN RAC 17 17-300-01
111-000085-	00	CONN AMPHENOL RT ANGLE PIN 17-1208-02
111-000086-	00	CONN AMPHENOL RT ANGLE PIN 17-1209-02
111-000087-	00	CONN COMPONENT LEAD SOCKET 380635-1
111-000088-	00	CONN EPO GROUND TAB 5271288
111-000089-	00	CONN TAPE LU9 BA14-8M
111-000090-	00	CONN TAPE LU9 BA16-8M
111-000091-	00	CONN PWR RECEPT. MS3102 A24-25
111-000092-	01	CON PLUG & CORD DLAMP 20A 2501
111-000093-	00	CONN BLOCK SKT 75 CONT AMP 201311-1
111-000094-	00	CONN BLOCK 29 POSN AMP 202477-4
111-000095-	00	CONN CONT SKT 18-16AWG AMP 66101-1
111-000096-	00	CONN CONT SKT 10-8AWG AMP 66257-2
111-000097-	00	CONN SKT RG/U CA AMP 329013
111-000098-	01	PIN LOCATING KEY 583532-1
111-000099-	00	CONN MINI BRASS RIVIT .116X3/16
111-000100-	00	CONN 24 PIN (PART # 111000040)
111-000101-	00	CONN CABLE 40 DUAL POSN AMP 1-86148-1
111-000102-	00	CONN PLUG RECP P&S TURNLOCK
111-000103-	00	CONN ASSY DIGITRONICS PTR 2540
111-000104-	00	CONN CRIMP LUG T&B RC1157
111-000105-	00	CONN RECTANGULAR MRAC 42SJ
111-000106-	00	CONN PIN CONTACT
111-000107-	00	CONN MOLEX STD NYLON P/N 126-P-1
111-000108-	00	CONN MOLEX STD NYLON P/N 1261-R
111-000109-	00	CONN MRAC 42PJ
111-000110-	00	CONN PIN CONTACT 8114
111-000111-	00	TERM R TNG #10 STUD 12-10 AMP 2-35109-1
111-000112-	00	CONN PCB 28 DUAL POSITION
111-000113-	00	CONN CABLE 20 POSN AMP 86402-1
111-000114-	00	CONN 12 POSITION AMP 86402-4
111-000115-	00	CONN CONTACT TWIN LEAF AMP 583616
111-000116-	00	CONN KEY AMP 583274
111-000117-	00	CONN PC EDGE 50 DUAL POS AMP 1-583717-9
111-000118-	00	CONN CINCH 252-15-30-160
111-000119-	00	CONN PC EDGE 10 DUAL POS AMP 583717-1
111-000120-	00	CONN FERRULE COAX 328664
111-000121-	00	CONN RETENTION SPRING COAX 243332-1
111-000122-	00	CONN ALIGN BSHG RED AMP 329051
111-000123-	00	CONN SPR RTNG AMP 583691-3
111-000124-	00	CONN RECEPTACLE MOLEX 1292-R2
111-000125-	00	CONN PIN FEMALE MOLEX 02091133
111-000126-	00	CONN PLUG MALE MOLEX 1292-P1
111-000127-	00	TERM MALE .093 18 TO 22 GA MOLEX 1380
111-000128-	00	CONN RIVET FLAT HD AK41H
111-000129-	00	CONN RECEPTACLE MOLEX 1261R-2
111-000130-	00	CONN PLUG MOLEX 1261P-1
111-000131-	00	CONN PIN MOLEX 02092132
111-000132-	00	CONN RF PNL RECEPTOR 83-798-1050
111-000133-	00	CONN JACKSCREW FEMALE 200875
111-000134-	00	CONN 9 PIN W/MOUNTING TABS
111-000135-	00	TERM FEM .093 18 TO 22 GA MOLEX 1381
111-000136-	00	CONN PLUG 2 PIN
111-000137-	00	CONN RECEPTACLE 2 PIN
111-000138-	00	CONN 22 PIN 583533-9
111-000139-	00	TERM SLTD TNG FLG #6 16-14A#2-320861-1
111-000140-	00	TERM R TNG #6 STUD 16-14 AMP 2-32442-1
111-000141-	00	TERM R TNG #8 STUD 22-16 AMP 2-31886-2
111-000142-	00	CONN MALE A/C PLUG 15 AMP 125V
111-000143-	00	CONN DAISY CHAIN .025 SQ POST 5"SP
111-000144-	00	TERM R TNG #2 STUD 22-16 AMP 2-320440-1
111-000145-	00	CONN FEMALE/D110238-35
111-000146-	00	CONN MALE/D110238-34
111-000147-	00	CONN 13 POS SINGLE ROW MOD IV
111-000148-	00	CONN KEY AMP 86286-1
111-000149-	00	CONN HOUSING, TWIN LLEAF .100CTRS
111-000150-	00	CONN AMP 225-21031-101 OR EQUIV
111-000151-	00	CONN CINCH 251-18-30-160
111-000152-	00	CONN AMP 57-30360
111-000153-	00	CONN FLAG FASTON TERM
111-000154-	00	CONN OUTPUT ELCO 00-8016-038-000-707
111-000155-	00	CONN BERG #75307-002
111-000156-	00	CONN JACKSCREW AMP #202490-2
111-000157-	00	CONN FLANGED INLET AH 5278 NEMA 5-15P
111-000158-	00	CONN WIRE MOLD ASSY 10P AMCO PM60-10
111-000159-	00	CONN RUBBER BOOTH AH 7511
111-000160-	00	CONN 30 PIN W/FRAME, VIKING #3VH30/LJN3
111-000161-		CONN WIRE MOLD ASSY 6 POS
111-000162-	00	CONN PIN CONTACT 14 AWG AMP 61118-5
111-000163-	00	CONN PIN CONTACT 26 AWG AMP 60910-5
111-000164-	00	CONN SOCKET AC ARROW HART #5278
111-000165-	00	CONN SOCKET AMP 61117-5
111-000166-	00	CONN CONT SKT 30-22 AWG AMP 60909
111-000167-	00	CONN 6 SKT MATE-N-LOK AMP 1-480273-0
111-000168-	00	CONN 12 SKT MATE-N-LOK AMP 1-480275-0
111-000169-	00	CONN 12 PIN MATE N-LOK AMP 1-480275-0
111-000170-	00	CONN PLUG MOLEX 12 CKT 1360P
111-000171-	00	CONN RCPT MOLEX 12 CKT 1360R-1

PART NUMBER	REV	DESCRIPTION
111-000172-	00	CONN VIKING 3VH30/1JN3
111-000173-	00	CONN AMP 57-30360
111-000174-	00	CONN MOLEX 5 PIN WAFERCON
111-000175-	00	CONN MOLEX 5 PIN
111-000176-	00	CONN BASELESS CRTG LAMP AMP 61528-1
111-000177-	00	TERM TAB 250 .130STD 2PR AMP 41481
111-000178-	00	CONN USM POP RIVET AD42S
111-000179-	00	CONN PC EDGE 25 DUAL POS AMP1-583717-1
111-000180-	00	CONN WIRE MOLD ASSY
111-000182-	00	CONN WIRE MOLD ASSY MODIFIED
111-000183-	00	CONN TEST PROBE FEM #53061
111-000184-	00	CONN TEST PROBE MALE #20357
111-000185-	00	CONN 50 DUAL POS
111-000186-	00	CONN AMP FSTON 187 SERIES TAB 61947-1
111-000187-	00	CONN AMP FSTON 187 SERIES TAB 61951-1
111-000188-	00	CONN AMP FSTON"187" RECP AMP 61697-1
111-000189-	00	CONN HOUSING MALE 9 PIN
111-000190-	00	CONN HOUSING FEMALE 9 PIN
111-000191-	00	CONN FASTON CLIP-FLAG TYPE
111-000192-	00	CONN BARRIER STRIP 6 TERMINAL
111-000193-	00	CONN SPADE LUG #10-12
111-000194-	00	CONN WAFER 9 PIN MOLEX 0918-5094
111-000195-	00	CONN AMP FSTON 110 TAB 42971-1
111-000196-	00	CONN AMP FSTON 187 TAB 61761-1
111-000197-	00	CONN 40 PIN W/STRAIN RELIEF #3417-3000
111-000198-	00	CONN 40 PIN PCB HEADER #3432-1002
111-000199-	00	CONN POLARIZING KEY
111-000200-	00	CONN VIKING 3VH35/1CND-12
111-000201-	00	TERM R TNG #4 STUD 22-16 AMP 31878
111-000202-	00	TERM R TNG #10 STUD 6 AWG AMP 52265-2
111-000203-	00	TERM RCPT 250 14-10 AWG 41450
111-000204-	00	CONN HSG 250 TERM RCPT AMP 1-480416-0
111-000205-	00	TERM RCPT 187 22-18 AWG AMP 60972-2
111-000206-	00	TERM RCPT 110 22-18 AWG AMP 61048-2
111-000207-	00	TERM TAB 187 130 STUD ANLR AMP 61761-2
111-000208-	00	TERM TAB 110 136 STUD STR AMP 60858-1
111-000209-	00	TERM POST 025SQ .165 AMP 87022-9
111-000210-	00	SPLICE COAX TO AWG AMP #330592
111-000211-	00	CONN BRASS RIVET TIN PLATED
111-000212-	00	CONN PNL RCPT TYPE UHF AMPHENOL 83-1R
111-000213-	00	TERM RCPT 28-22 AWG BERG 47712
111-000214-	00	CONN HSG 4 PIN BERG 65039-033
111-000215-	02	CONN 3VH50/1JV5 VIKING
111-000216-	00	TERM R TNG #8 STUD 16-14 AMP 30927
111-000217-	00	CONN RECEPTACLE MOLEX #1261-R2
111-000218-	00	CONN PLUG MOLEX #1261-P
111-000219-	00	CONN 9 PIN MOLEX #1840-9-2
111-000220-	00	CONN 12 PIN MOLEX #1840-12-2
111-000221-	00	CONN QUICK DISC TAB ETC #3531
111-000222-	00	CONN QUICK DISC TAB ETC #3523
111-000223-	00	CONN 25 PIN DUAL POSN #PJDH-25S
111-000224-	00	CONN POLARIZING KEY #109-8597
111-000225-	00	TERM R TNG #10 STUD 6 AWG BUR YAEUSC-L1
111-000226-	00	TERM RCPT 250 14-10 AWG BUR PQ10R258B
111-000227-	00	CONN 29 PIN WINCHESTER #SRE29PD4J
111-000228-	00	CONN MR 4 PIN HDR (TIN) AMP #9-350255-1
111-000229-	00	CONN MR 4 SKT HSG AMP #1-350240-9
111-000230-	00	CONN MR 6 PIN HDR (TIN) AMP #9-350258-1
111-000231-	00	CONN MR 6 SKT HSG AMP #1-350241-9
111-000232-	00	CONN MR 9 PIN HDR (GOLD) AMP #9-350261-2
111-000233-	00	CONN MR 9 SKT HSG AMP #1-350242-9
111-000234-	00	CONN MR 12 PIN HDR (TIN) AMP #9-350264-1
111-000235-	00	CONN MR 12 SKT HSG AMP #1-350243-9
111-000236-	00	CONN MR SKT CON 26-18 TIN AMP 350037-1
111-000237-	00	CONN MR SKT CON 26-18 GLD AMP 350037-2
111-000238-	00	CONN HOUSING AMP 1-480305-0
111-000239-	00	CONN PIN AMP 61118-1
111-000240-	00	CONN PIN MALE 20-14 MOL3X #20-09-2101
111-000241-	00	CONN PIN FEMALE 20-14 MOLEX #20-09-1101
111-000242-	00	CONN 60 PIN AMP 582459-1
111-000243-	00	CONN PIN MALE 22-18 MOLEX #02-09-2116
111-000244-	00	CONN PIN FEMALE 22-18 MOLEX #02-09-1116
111-000245-	00	CONN PLUG FOR .093 TERM MOLEX TYPE 1619
111-000246-	00	CONN RCPT FOR .093 TERM MOLEX TYPE 1619
111-000247-	00	CONTACT, CONN. AMP #66135-2
111-000248-	00	SHIELD, CONN. AMP #200532-1
111-000249-	00	JACKSCREW AMP #582360-3
111-000250-	00	CONNECTOR, DUAL, 36 PIN 600-061-18SL
111-000251-	00	CONNECTOR 582388-9 AMP
111-000252-	00	CONTRACT, CONN. 66088-3 AMP
111-000253-	00	CONTRACT, CONN. 66150-3 AMP
111-000254-	00	CONNECTOR WINCHESTER #MRAC50PJTDH8
111-000255-	00	CONN W/FRAME, CINCH #251-25-30-160
111-000256-	00	CONNECTOR 57-30240
111-000257-	00	CONN CARD CAGE-TERMINAL
111-000258-	00	CONN CARD CAGE 15 PIN
111-000259-	00	CONN MR 15 PIN HDR (TIN) AMP #9-350267-1
111-000260-	00	CONN MR 15 SKT HSG AMP #1-35024409
111-000261-	00	CONN PIN .025SQ,WW,.660LG #75401-015
111-000262-	00	CONN CANNON 19S SK-19-21C-1/2
111-000263-	00	CONN PC QUICK-CONNECT .187 TAB FEMALE
111-000264-	00	TERM R TNG #6 STUD 18-22 AMP 2-34144-1
111-000265-	00	TERM R TNG #6 STUD 10-12 AMP 2-34168-1
111-000266-	00	CONN RIVET
111-000267-	00	CONN FEMALE MOLEX 1189T PIN
111-000268-	00	CONN MALE MOLEX 1380T
111-000269-	00	CONN MALE MOLEX 1120T PIN
111-000270-	00	CONN FEMALE PIN MOLEX 1381T
111-000271-	00	CONN USM POP RIVET #AD44H
111-000272-	00	TERM POST .025SQ UMINSUL. AMP #87022-4
111-000273-	00	TERM AMP 250 FASTON ADT 61765-2
111-000274-	00	CONN KEY, POLARIZING FOR AMPMODU TYPE
111-000275-	00	CONN CONTRACT, LOCK CLIP -.025 POST
111-000276-	00	CONN HOUSING, LOCK CLIP, 2 ROW 6 POS
111-000277-	00	CONN HOUSING, LOCK CLIP, 2 ROW 20 PCS
111-000278-	00	CONN PLDG 20A 250V HUBBELL 2421
111-000279-	00	CONN AMP PINS (BRIGHT TIN DIP)
111-000280-	00	CONN RCPT 2-PIN MOLEX #03-:9-1021
111-000281-	00	CONN SCREW LOCK PNL RECEPTACLE
111-000282-	00	CONN SCREW LOCK CA PLUG
111-000283-	00	CONN MATE-N-LOCK 8 PIN HDR, #350212-1
111-000284-	00	CONN MATE-N-LOCK 8 PIN, AMP #1-480283-0
111-000285-	00	CONN 20-14 TIN PIN, AMP #60619-1
111-000286-	00	CONN POST INSUL POD AMP #1-480306-1
111-000287-	00	CONN FLAG INSUL SPT AMP #60290-2
111-000288-	00	CONN WINCHESTER HW50D2-111-2B
111-000289-	00	TERM MALE-MOLEX 1854-02-06-2132
111-000290-	00	TERM RECEP,2 CKT MOLEX 1625-2R1
111-000291-	00	CONN ADPTR 1/4" PUSHON TAB-1:2
111-000292-		CONN HOUSING, LOCK CLIP 12 POS
111-000293-	00	CONN 11 POS 22 PIN, EDGE CARD
111-000294-	00	CONN 4 PIN MR HDR (GOLD) AMP-9-350255-2
111-000295-	00	CONN 15 PIN MR HDR (GOLD) AMP -9-350267-2
111-000296-	00	CONN 20-14 GOLD PIN TP DR AMP 60619-5
111-000297-	00	CONN M-N-L 8 PIN HDR GLD AMP #350212-2
111-000298-	00	CONN HSG 50 DUAL POS, AMP #1583717-7
111-000299-	00	CONN 50 POS. 4 SURF DISK 3426-0000 3M
111-000300-	00	CONN 25 POS. 4 SURF DISK 3415-0000 3M
111-000301-	00	CONN 34 POS. 4 SURF DISK 3M P/N 3402
111-000302-	00	CONN 34 POS. 4 SURF DISK 3M 3424
111-000303-	00	TERM .250 INLINE FEM N2/4-2/10
111-000304-	00	TERM INSUL-CONNECT 18-20 GA WIRE
111-000305-	00	CONN AMP FASTON 45 250 SER SGL 42822-2
111-000306-	00	CONN AMP FASTON 45 250 SER DBL 41477
111-000307-	00	CONN CONT TWINLEAF AMP 583853-5
111-000308-	00	CONN 22 PIN W/FRAME, VIKING #3VH22/LJN3
111-000309-	00	CONN FASTON 14-20 AWG NON-INSUL 42452-2
111-000310-	00	CONN 18 CONT SINGLE ROW 00000032
111-000311-	00	CONN 18 CONT DUAL POS 00000033
111-000312-	00	CONN 18 CONT DUAL POS HSG 00000029
111-000313-	00	CONN OUTPUT J2 M600L 00000028
111-000314-	00	CONN CONT MALE PIN 22-26 AWG
111-000315-	00	CONN CONT FEM SKT PIN 22-26 AWG
111-000316-	00	CONN 250 FASTON 10-20 AWG TERM 350563
111-000317-	00	CONN 75 POS M SER 100 MBYTE
111-000318-	00	CONN W /FRM CINCH 251-22-30-160
111-000319-	00	CONN PLUG 30A 250V HUBBELL 45215
111-000320-	00	CONN 50 POS M SERIES 100 MBYTE
111-000321-	00	CONN CONTACT 15 AMP 1332
111-000322-	00	CONN PWR POLE MDL 15 AMP 600V 1315
111-000324-	00	CONN WAFERCON 3 PINS MOLEX 09-18-5031
111-000325-	00	CONN TWIST LOCK 30A 125/250V 2713
111-000326-	00	CONN TWST-LCK 30A 125/250V 2715
111-000327-	00	CONN ASSY DIGITRONICS BC7611-2 22 PINS
111-000328-	00	CONN DEAD FRONT CAP 15A 250V N2 5666C
111-000329-	00	CONN 29 PIN SOCKET SRE-29S-JT
111-000330-	00	TERM PRE-INSUL #6 WIRE AMP 52042-3
111-000331-	00	CONN 9 CONT PLUG DEC9PW/O PINS
111-000332-	00	CONN 9 CONT SKT DEC9SW/O PINS
111-000333-	00	CONN 25 CONT PLUG DBC25P W/O PINS
111-000334-	00	CONN 25 CONT SKT DBC25S W/O PINS
111-000335-	00	CONN 50 CONT PLUG DDC50P W/O PINS
111-000336-	00	CONN 50 CONT SKT DDC50S W/O PINS
111-000337-	00	CONN 19 CONT PLUG 2DE19P W/O PINS
111-000338-	00	CONN 19 CONT SKT 2DE19S W/O PINS
111-000339-	00	CONN 52 CONT PLUG 2DB52P W/O PINS
111-000340-	00	CONN 52 CONT SKT 2DB52S W/O PINS
111-000341-	00	CONN 100 CONT PLUG 2DD100P W/O PINS
111-000342-	00	CONN 100 CONT SKT 2DD100S W/O PINS
111-000343-	00	CONN CONT TW LF 20-24AWG AMP 583853-2
111-000344-	00	CONN TWIST LOCK HUBBELL 2313
111-000345-	00	CONN TWIST LOCK CAP HUBBELL 2311

PART NUMBER	REV	DESCRIPTION
111-000346-	00	CONN TWIST LOCK INLET HUBBELL 2315
111-000347-	00	CONN 1 POLE MTG PLATE ITE FP9508
111-000348-	00	CONN 2 POLE MTG PLATEITE FP9555
111-000349-	00	CONN 3 POLE MTG PLATE ITE FP9556
111-000350-	00	CONN SEAL-TITE CVR HUBBELL 6031
111-000351-	00	CONN SEAL-TITE CVR HUBBELL 6032
111-000352-	00	CONN SEAL-TITE CVR HUBBELL 6035
111-000353-	00	CONN SEAL-TITE CVR HUBBELL 6021
111-000354-	00	CONN CAP TWIST LOCK 30A 125/250V 2711
111-000355-	00	CONN RCPT DUPLEX 20A 125V 5392
111-000356-	00	CONN RCPT SGL 20A 125V 5361
111-000357-	00	CONN PLZ SKT 203964-2
111-000358-	00	CONN PLZ PIN 200833-4
111-000359-	00	CONN JACKSCREW FIXED FEM 200875-1
111-000360-	00	CONN PLZ SKT 201047-4
111-000361-	00	CONN PLZ PIN 201046-4
111-000362-	00	CONN JACKSCREW FIXED MALE 200874-2
111-000363-	00	CONN SKT PIN PCB 85861-4 AMP
111-000364-	00	CONN INLET 3 WIRE 30A 250V 2625
111-000365-	00	CONN 3 WIRE 30A 250V 2623
111-000366-	00	CONN PLUG 3 WIRE 30A 250V 2621
111-000367-	00	CONN FASTON 3
111-000367-	00	CONN FASTON 45DEG MALE 42822-2
111-000368-	00	CONN 25/50 PIN CD EDGE 3415-25
111-000369-	00	CONN 34 PIN W/W POST 3424
111-000370-	00	CONN R/W HD 5 PIN FEMALE 13540
111-000371-	00	CONN 22/44PIN CD EDGE .125" CTRS
111-000372-	00	TERM PRE INSULATED #8AWG 52263-1 AMP
111-000373-	00	TERM BARRIER STRIP 2 PIN 99999-026
111-000374-	00	TERM BARRIER STRIP 6 PIN 99999-027
111-000375-	00	CONNECTOR 22 PIN CUSTOM 01021-006
111-000376-	00	CONN PLUG 52-66-C CAB ASSY
111-000377-	00	CONN 14P DIP SKT FINISH TIN 583527-1
111-000378-	00	TERM BLOCK END SECTION 230V
111-000379-	00	TERM BLOCK SECTION HD PN
111-000379-	00	TERM BLOCK SECTION HD PHNLC 212
111-000380-	00	CONN 50/100 PIN CARD EDGE CPH70000
111-000381-	00	CONN BUS BAR 6 1/2" 98438 1100 SERIES
111-000382-	00	CONN HSG LOCK CLIP 2 ROW 8 POS
111-000383-	00	CONN RECEPT BRN PHEN DPLX 15A 125V
111-000384-	00	PLUG 50A 3P 3 WIRE 3761
111-000385-	00	PLUG 50A 3P 4 WIRE 3765
111-000386-	00	CONN FLANGED INLET 50A 3P 4 WIRE 3775
111-000387-	00	CONN BODY 50A 3P 4 WIRE 3764
111-000388-	00	CONN INLET 50A 3P 3 WIRE 3776
111-000389-	00	CONN BODY 50A 3P 3 WIRE 3760
111-000390-	00	CONN PWR POLE MDL 15 AMP 600V 1327
111-000391-	00	TERM RCPT 28-32AWG BERG 47711
111-000392-		TERM JUMPER PINS 8136-650
111-000393-	00	CONN PLUG CORR-RESIST 30A 125V 26CM11
111-000394-	00	CONN BODY CORR-RESIST 30A 125V 26CM13
111-000395-	00	CONN SEAL TITE CVR 60CM31
111-000396-	00	CONN SEAL TITE CVR W/RING 60CM33
111-000397-	00	CONN PWR INLET 30A 125V60CM61
111-000398-	00	TERM 4 STRIP THRU CHAS 4-140Y
111-000399-		CONN PLUG, FEMALE DF21YC
111-000400-		CONN PLUG, FEMALE PF21GNC
111-000401-		TERMINAL 269RR
111-000402-		TERMINAL 269BB
111-000403-		TERMINAL 1519
111-000404-		TERMINAL 257
111-000405-		CONN PLUG, F 15A 50HZ 377-R1
111-000406-		CONN PLUG, MALE PS100GB
111-000407-		CONN PLUG, MALE PS25GWT
111-000408-		CONN PLUG, MALE PS25GGN
111-000409-		CONN PLUG, MALE PS25GR
111-000410-		CONN PLUG, MALE PS100GR
111-000411-		CONN PLUG, FEMALE RP25GY
111-000412-		CONN PLUG, FEMALE DF21RC
111-000413-		CONN PLUG, FEMALE DF21WTC
111-000414-		CONN PLUG, FEMALE DF21BC
111-000415-		CONN PLUG, FEMALE RP100GB
111-000416-		CONN PLUG, FEMALE RP25GBL
111-000417-		CONN PLUG, FEMALE RP25GWT
111-000418-		CONN PLUG, FEMALE RP25GGN
111-000419-		CONN PLUG, FEMALE RP25GR
111-000420-		CONN PLUG, FEMALE RP100GR
111-000421-		CONN PLUG, MALE PS25GBL
111-000422-	00	TERM R TNG 1/4STD 22-16 AMP 31251
111-000423-		CONN PLUG M TWIST LOCK 20A 125V 60HZ
111-000424-		CONN RCPT F 4X 220V 50HZ
111-000425-		CONN RCPT F 4X 110V 60HZ
111-000426-	00	CONN 2P POS AMP 9-350359-2
111-000427-		CONN 50POS WINCHESTER HW25C2-111
111-000428-	00	CONN N/R 12PIN HDR 3/32 GOLD 93502662
111-000429-	00	CONN CKT CD HDR 34 CONT STR 3431-2003
111-000430-	00	CONN FLAG SLIP-ONS 10-12AWG S09415
111-000431-	00	CONN COMP LEAD SKT 380598-2
111-000432-	01	CONN DIABLO M44 I/O CONN
111-000433-		CONN 3VH22/1JN3
111-000434-		CONN IC TST SKT
111-000435-	00	TERM INSUL 4099-1 05-19 TEFLON
111-000436-	00	CONN PLUG 15A 250V PVC 5666
111-000437-	00	CONN SOCKET CONTRACT WIN MRAC 50SJTDH
111-000438-	00	CONN GOLD PIN-FEMALE MOLEX
111-000439-	00	CONN GOLD PIN-MALE (PC TAIL) MOLEX
111-000440-	00	TERM SPADE LUG .196 (@10ADW) 626
111-000441-	00	TERM SPADE LUG .257 (1/4") 571
111-000442-	00	CONN RECPT ELECT 250V 15A DPLX 5662
111-000443-	00	CONN RECEP MOLEX 9 PIN 0309-1093
111-000444-	00	CONN RECPT. 9 PIN MOLEX 03-09-1094
111-000445-	00	CONN RCPT AC AMP1-480700-0 CD83435302
111-000446-	00	CONN PINS AC AMP 350550-1 CD83435510
111-000447-		CONN 14 PIN DIABLO 10524-11
111-000448-		CONN PIN-MALE DIABLO 10525-10
111-000449-	00	CONN ELCO 20 DUAL POS CARD EDGE CONN
111-000450-	00	CONN PLUG STR BL 50A 125/250V 9451
111-000451-		TERM SOCKET #66108-3

PART NUMBER	REV	DESCRIPTION
113-000001-	00	CB 10A 65V MAX AIRPAX APG1-1
113-000002-	00	FUSE 10A 250V LITTLEFUSE 3AB#314010
113-000003-	00	FB 2-POLE, 3AG MTG, LITTLEFUSE #357002
113-000005-	00	FUSE 3/4A 250V LITTLEFUSE 8AG#361.750
113-000007-	00	FUSE 3/4A FAST ACTING
113-000008-	00	FUSE CLIP, EARLESS, BUSS #5680-05
113-000009-	00	FUSE 2A 250V LITTLEFUSE 8AG#361002
113-000010-	00	FUSE 3A 125V LITTLEFUSE 3AG#313003
113-000011-	00	FUSE 2A 125V LITTLEFUSE 3AG#313002
113-000012-	00	FUSE 1/2A 125V LITTLEFUSE 3AG#313.500
113-000013-	00	FUSE 3/8A 250V BUSS MDL FUSETRON
113-000014-	00	FUSE 1A 250V BUSS AGX FAST ACTING
113-000015-	00	FUSE 4A 250V LITTLEFUSE 3AG#312004
113-000016-	00	CB 15A 50V 1-POLE TI#51MC2-29-15
113-000017-	00	FUSE 15A 32V LITTLEFUSE 1AG#301015
113-000018-	00	FUSEHOLDER PNL MTD,R-A TERM,LF#342004
113-000019-	00	FUSE 15A 250V LITTLEFUSE 3AB#314015
113-000020-	00	FUSE 30A 600V BUSS KTK LIMITRON
113-000021-	00	FUSE BLOCK 3-POLE 250V BUSS #2809
113-000022-	00	FUSE 5A 32V LITTLEFUSE 1AG#301005
113-000023-	00	FUSE 10A 32V LITTLEFUSE 1AG#301010
113-000025-	00	FUSEHOLDER PNL MTD,STR TERM,LF#342012
113-000026-	00	FUSE 30A 125V LITTLEFUSE 3AB#314030
113-000027-	00	FUSEHOLDER PNL MTD,H-V KNOB, LF#340276
113-000028-	00	PICOFUSE AX LEAD 3/4A 125V LF#275.750
113-000029-	00	FUSE 2 1/2A 32V BUSS AGW GLASS TUBE
113-000030-	00	FUSE 1/4A 250V BUSS AGX FAST ACTING
113-000032-	00	FUSE 15A 32V BUSS MDL FUSETRON
113-000033-	00	FUSE 5A 250V LITTLEFUSE 3AB#314005
113-000034-	00	FUSE 1A 32V BUSS AGA GLASS TUBE
113-000035-	00	FUSE 3A 32V BUSS AGA GLASS TUBE
113-000036-	00	FUSE 6A 32V BUSS AGA GLASS TUBE
113-000037-	00	FUSE 8A 250V LITTLEFUSE 3AB#314008
113-000038-	00	FUSEHOLDER PNL MTD,STR TERM,LF#342038
113-000039-	00	PICOFUSE (REPLACED BY 113000028)
113-000040-	00	FUSE 15A 32V BUSS AGC FAST ACTING
113-000041-	00	FUSE 2A 250V LITTLEFUSE 3AG#312002
113-000042-	00	PICOFUSE AX LD,1 1/2A 125V,LF#26501.5
113-000043-	00	FUSE 5A 32V BUSS MDL FUSETRON
113-000044-	00	FUSE 3A 32V LITTLEFUSE 1AG#301003
113-000045-	00	FUSE 4A 32V BUSS AGW FAST ACTING
113-000046-	00	CB 20A 65V 2P AIRPAX #UPG11-2746-1
113-000047-	00	FUSE 5A 125V LITTLEFUSE 3AG#313005
113-000048-	00	FUSEHOLDER IN LINE FOR 3AG
113-000049-	00	FUSEHOLDER, MODIFIED, IN LINE FOR 3AG
113-000050-	00	FUSE 1/4A 250V LITTLEFUSE 3AG#313.250
113-000051-	00	FUSE .125A BUSS MDL SLO BLO
113-000052-	00	FUSE 4A 32V LITTLEFUSE 3AG#311004
113-000053-	00	FUSE 5A 32V LITTLEFUSE 3AG#311005
113-000054-	00	FUSE 10A 32V LITTLEFUSE 3AG#311010
113-000055-	00	CB 8A 50160HZ 250V AIRPAX 00000188
113-000056-	00	FUSE 1A SLO BLO 3AG 313001
113-000057-	00	FUSE 1A 250V LITTLEFUSE 3AG#312001
113-000058-	00	FUSE 1/8A 3AG 2310 800316-001
113-000059-	00	FUSE 8A USE 113-37 2310 800316-150
113-000060-	00	FUSE 15A USE 113-19 2310 800316-150
113-000061-	00	FUSE 1/2A 250V 3AG LITTLEFUSE 312.500
113-000062-	00	FUSE 3A 125V 203115401
113-000063-	00	FUSE 2A 250V 203115305
113-000064-	00	CB 3POLE 20A 209-3-1-62F-3-8-20
113-000065-	00	CB 2POLE 20A 209-2-1-62F-3-8-20
113-000066-	00	CB 1POLE 20A 209-1-1-62F-3-8-20
113-000067-	00	CB 4POLE 20A 209-4-1-62F-3-8-20
113-000068-	00	FUSE 5A PICOFUSE 125V 275005
113-000069-	00	CB 10A 4 POLE CAB 230V
113-000070-	00	CB 10A 3 POLE 230V CAB
113-000071-	00	CB 10A 2 POLE CAB 230V
113-000072-	00	FUSE 1A 125V 3AG 00000633
113-000073-	00	FUSEHOLDER 00000594
113-000074-	00	CKT BREAKER 3A 250V 00000593
113-000075-	00	CB 6P 10A,10A,10A,10A,15A,15A
113-000076-	00	CB 4P 10A,10A,15A,15A 209-4-3417-1
113-000077-	00	CB 2P 15A CD2-A3-DU-15-240-60-2
113-000078-	00	CB 4P 20A,20A,20A,10A 209-4-3415-1
113-000079-	00	CB 3P 20A,20A,10A 209-3-3414-1
113-000080-	00	CM BOOT 2 POLE 1113/34 OR 006-10196
113-000081-		CB 3A 50VDC 431-203-101
113-000082-		CB 15A 250V 60HZ 512-215-101
113-000083-		CB 10A 109-210-101
113-000084-		CB 25A 109-225-101
113-000085-		CB 30A 109-230-101
113-000086-		CB 35A 109-235-101
113-000087-	00	CB PANEL DIST BREAKER 11499
113-000088-	00	FUHLR PNL LITTLEFUSE #342028
113-000089-	00	FUSE LINE 1A 250V 3AG 313001
113-000090-	00	FUHLR FUSE CLIP 391
113-000091-	00	FUSE 8A SLO BLO BUSS 7DA8
113-000092-	00	FUSE PICO 2A 125V 275002
113-000093-	00	FUSE PICO 4A 125V 275004
113-000094-	00	CB 3P 20A, 15A, 15A, 209-3-3684-1
113-000095-	00	CB 4P 15A, .15A, 20A, 20A 20.-4-3683-U
113-000096-	00	CB 4P 20A, .20A, 15A, 15A 209-4-3684-1
113-000097-	00	CB 6P 15A, .15A, 15A, 15A, 20A, 20A
113-000098-	00	CB 5P 20A,20A,20A,15A,15A 209-5-3686-1
113-000099-	00	CB SWITCH 230V 50HZ
113-000100-	00	CB SWITCH 115V 60HZ
113-000101-	00	FUSE 3A8 314003

PART NUMBER	REV	DESCRIPTION
114-000001-	00	HUDSON 28V BULBS 2187D
114-000002-	00	HUDSON BULB 2176
114-000003-	00	INDICATOR CARTRIDGE CML 640321
114-000004-	00	INDICATOR CARTRIDGE CML
114-000005-	00	INDICATOR CARTRIDGE CML 64 0272
114-000006-	00	INDICATOR CARTRIDGE 6V CML 240272 GR W
114-000007-	00	INDICATOR CARTRIDGE 115V CML 240321 RE
114-000008-	00	LAMP TUNGSOL #561
114-000009-	00	BULB-PLT LAMP CML 84-0421
114-000010-	00	LAMP PILOT 115V NEON (SEE 114000009)
114-000011-	00	LAMP INCANDESCENT AMBER 14V
114-000012-	00	LAMP INCANDESCENT RED 14V
114-000013-	00	INDICATOR RDOUT DIG SP-331 1.5D16.33"
114-000014-	00	INDICATOR RDOUT DIG SP-32
114-000014-	00	INDICATOR RDOUT DIG SP-332 2DIG.33 IN
114-000015-	00	INDICATOR RDOUT DIG SP-333 3DIG.33 IN
114-000016-	00	INDICATOR RDOUT DIG SP-353 3DIG.55 IN
114-000017-	00	INDICATOR RDOUT DIG SP-354 2.5D.55 IN
114-000018-	00	LAMP GE 379 37353790
114-000019-	00	INDICATOR FILE PROJECT 100105-002
114-000020-	00	BULB LIGHT BULB 10545
114-000021-	00	LAMP INCAND GV .20A 00000318
114-000022-	00	LAMP GE 1638 TLNBE0009
114-000023-	00	LAMP 302005102
114-000024-	00	LAMP 302104001
114-000025-	00	LAMP INDICATOR 800163-002
114-000026-	00	LAMP INDICATOR 2230 800785-002
114-000027-	00	LAMP LED VISIBLE 2230 801082-001
114-000028-	00	LAMP UV 4000W 10862
114-000029-	00	BULB GE 683 5V .06A 525372001
114-000030-	00	LAMP INCANDESCENT 060-419
114-000031-	00	LAMP INCANDESCENT 060-434
114-000032-	00	LAMP ASSY INCAND 5V 00000312
114-000033-	00	LAMP INCAN 6V .20A T1-3/4 00000318
114-000034-	00	INDICATOR LAMP 800163-003
114-000035-	00	BULB LAMP 6-3V RED CML-240271
114-000036-	00	BULB LAMP 6:3V GRN CML-240272
114-000037-		INDICATOR LIGHT 32R
114-000038-	00	LAMP ASSY OUTLINE CTG DISK 200-7236
114-000039-	00	BULB GE337
114-000040-	00	BULB HI-INTENSITY 6V 15W FM 150521
114-000041-		
114-000042-	00	LAMP G.E. 16651F
114-000043-	00	LAMP BASE 4345-006-UP

REV. 03

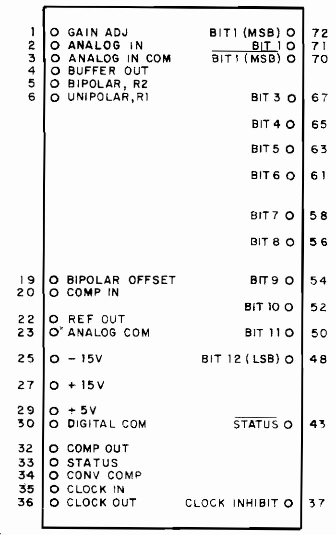
PART NUMBER	REV	DESCRIPTION
115-000001-	·00	FAN AXIAL-PAMOTOR 8500
115-000002-	·00	FAN AXIAL-ROTROMMUFFIWMK4
115-000003-		MOTOR DISC DRIVE
115-000004-	·00	BLOWER AMCO B-350-25 BS-350 2REQD BHA
115-000005-	·00	FAN ROTRON SARGENT 115V 50/60
115-000006-	·03	MOTOR DRIVE
115-000007-	·01	MOTOR HEAD LOAD
115-000008-	·00	FAN, SKIPPER
115-000009-	00	MOTOR DRIVE 50HZ
115-000010-	·01	MOTOR DRIVE 60HZ DISC 6000
115-000011-	·04	MOTOR CAPSTAN OUTLINE DWG
115-000012-	·04	MOTOR REEL OUTLINE DWG
115-000013-	00	MOTOR UNMODIFIED 3M103 GRANGER
115-000014-	·03	MOTOR SHADED POLE TRIEM 1012
115-000015-	00	BLOWER ADPT BRKT
115-000016-	·00	MOTOR FILTER (350 CFM)
115-000017-	·00	MOTOR SCREEN OUTLET (350 CFM)
115-000018-	·00	MOTOR AIR DUCT (350 CFM)
115-000019-	00	MOTOR ALUM GRILL
115-000020-	·00	BLOWER (350 CFM)
115-000021-	00	FAN SKIPPER ROTON #SK2A-1
115-000022-	·00	FAN ADAPTER, AIR DUCT
115-000023-	00	FAN 105 CFM HOWARD #3-90-8010-115V
115-000024-	·02	BLOWER LAMB #115721-0
115-000025-	01	MOTOR 1/3 HP GE#5KCP19PG285T
115-000026-	00	BLOWER AUXILLARY
115-000027-	00	BLOWER AUXILLARY 230V
115-000028-	·01	MOTOR HYSTERESIS SYNCH SPEC
115-000029-	00	FAN, VENTURI 115V,50/60HZ ROTRON CT3A2
115-000030-	·00	GUARD,FINGER ROTRON 20132-2
115-000031-	01	BLOWER SPEC CABINET 115V 50/60HZ
115-000032-	·00	MOTOR MAIN 101/A 525836001
115-000033-	00	MOTOR DRIVE 101/A 63002402-1
115-000034-	00	MOTOR 1.6A 60HZ UP ASR 33 182241
115-000035-	·00	BLOWER WIND JAMMER MGOOL 00000541
115-000036-	00	FAN COOLING 117V 60HZ 20237301
115-000037-	00	MOTOR ASSY BLOWER M600L 00001093
115-000038-	00	MOTOR ASSY SP-8 M600L 00001101
115-000039-	00	MOTOR BRUSH DRIV CDS 114 91528-001
115-000040-	00	MOTOR DRUM 2310 800899-001
115-000041-	00	MOTOR RIBBON 2310 800264-001
115-000042-	00	FAN 2310 800131-001
115-000043-	00	MOTOR 115V 50/60HZ 150086001
115-000044-	00	MOTOR 230V 50/60HZ 150086002
115-000045-	00	MOTOR DRIVE 900RPM 115 V VACCT381-2
115-000046-	02	BLOWER SPEC CABINET 230V 50HZ
115-000047-	00	MOTOR ASSY CC7073-6
115-000048-	00	MOTOR SPINDLE ASSY DIABLO 15536-02
115-000049-	00	MOTOR 50/60HZ 115V 327000001
115-000050-	00	MOTOR HD POS SYS 4 SURF DISK
115-000051-	00	MOTOR SYNCH SPECIAL 4 SURF DISK
115-000052-	00	MOTOR RIBBON 2230 801148-001
115-000053-	00	MOTOR DRUM MOTOR 2230 800954-001
115-000054-	00	MOTOR PAPER FD MOTOR ASSY 235145-001
115-000055-	00	MOTOR BLOWER 2230 80117-001
115-000056-	00	MOTOR TTY ASR 33 181870
115-000057-		MOTOR DRIVE 60HZ
115-000058-		MOTOR DRIVE 50HZ
115-000059-	00	MOTOR 60HZ BRPE-11 TTY 151795
115-000060-	00	MOTOR DRUM CDS 114 90074-001
115-000061-	00	MOTOR FAN ASSY 32810000
115-000062-	00	MOTOR DRIVE MOTOR ASSY 30136703
115-000063-	00	MOTOR PICK MOTOR ASSY 30136805
115-000064-	00	BLOWER COLLINS FAN ASSY 32810000
115-000065-	00	BLOWER AIR COND 115V 60HZ
115-000066-	00	BLOWER HEAT EXCHANGER 115V 50/60HZ
115-000067-	00	MOTOR NOVADISC DRIVE 6004-1,-2
115-000068-	00	MOTOR NOVADISC DRIVE 6004
115-000069-	00	BLOWER HEAT EXCHANGER 230V 50/60HZ
115-000070-	00	BLOWER AIR COND 230V 50/60HZ
115-000071-	00	BLOWER MOTOR 91185-001
115-000072-	00	MOTOR SPINDLE ASSY 97721-003
115-000073-	00	MOTOR BRUSH MOTOR 44 16023
115-000074-	00	MOTOR SPINDLE ASSY 44 16117
115-000075-	00	MOTOR BLOWER 2400 RPM 44 16099

NUMERICAL INDEX
CIRCUIT MODULES

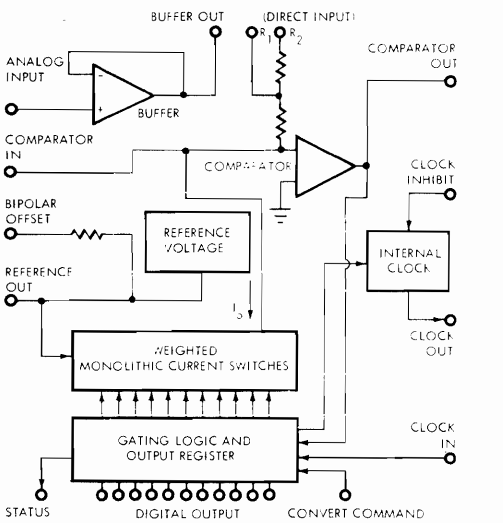
116000001

A/D Converter

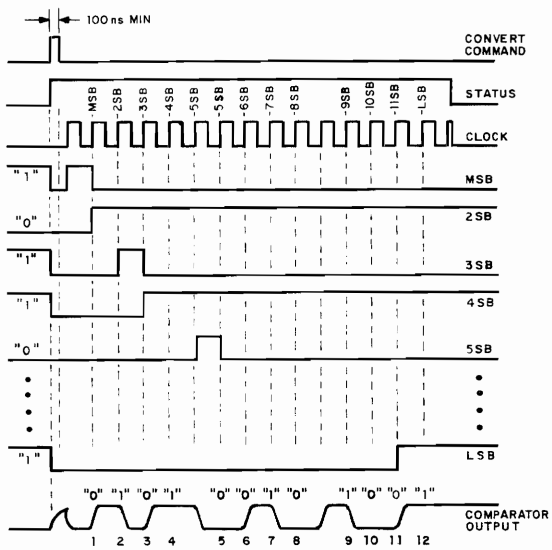
Pin Configuration
Top View



Block Diagram



Timing Diagram



Pin Designations

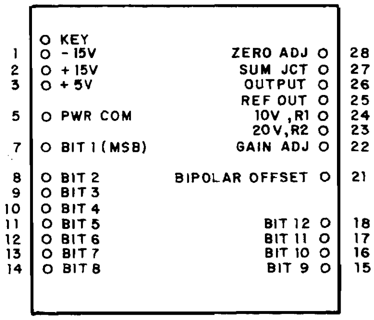
Pin No.		Pin No.	
1	Gain Adj.	72	Bit 1 (MSB)
2	Analog In	71	Bit 2
3	Analog In Com	70	$\overline{\text{Bit 1 (MSB)}}$
4	Buffer Out	69	No pin
5	Bipolar, R2	68	No pin
6	Unipolar, R1	67	Bit 3
7	No pin	66	No pin
8	No pin	65	Bit 4
9	No pin	64	No pin
10	No pin	63	Bit 5
11	No pin	62	No pin
12	No pin	61	Bit 6
13	No pin	60	No pin
14	No pin	59	No pin
15	No pin	58	Bit 7
16	No pin	57	No pin
17	No pin	56	Bit 8
18	No pin	55	No pin
19	Bipolar Offset	54	Bit 9
20	Comp In	53	No pin
21	No pin	52	Bit 10
22	Ref Out	51	No pin
23	Analog Com	50	Bit 11
24	No pin	49	No pin
25	-15V	48	Bit 12 (LSB)
26	No pin	47	No pin
27	+15V	46	No pin
28	No pin	45	No pin
29	+5V	44	No pin
30	Digital Com	43	$\overline{\text{STATUS}}$
31	No pin	42	No pin
32	Comp Out	41	No pin
33	Status	40	No pin
34	Conv Comm	39	No pin
35	Clock In	38	No pin
36	Clock Out	37	Clock Inhibit

The 116000001 circuit module is a 12-bit binary analog-to-digital converter.

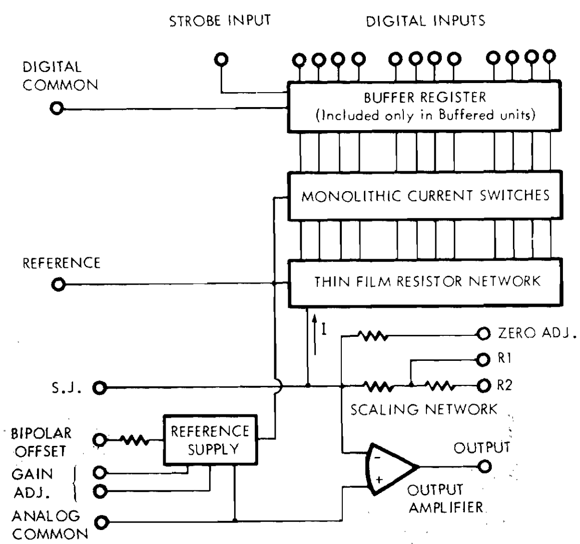
116000002

Pin Configuration

Top View



Block Diagram



D/A Converter

Pin Designations

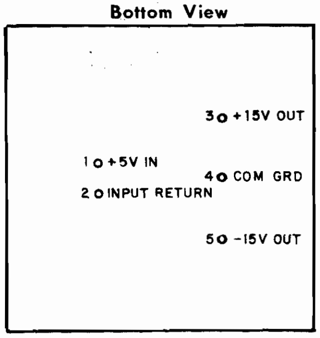
Pin No.	
K	Key
1	-15V
2	+15V
3	+5V
4	No pin
5	Pwr Com
6	No pin
7	Bit 1 (MSB)
8	Bit 2
9	Bit 3
10	Bit 4
11	Bit 5
12	Bit 6
13	Bit 7
14	Bit 8
15	Bit 9
16	Bit 10
17	Bit 11
18	Bit 12
19	No pin
20	No pin
21	Bipolar Offset
22	Gain Adj
23	20V
24	10V
25	Ref
26	Output
27	Sum JCT
28	Zero Adj

The 116000002 circuit module is a 12-bit binary digital-to-analog converter with an externally programmable output amplifier.

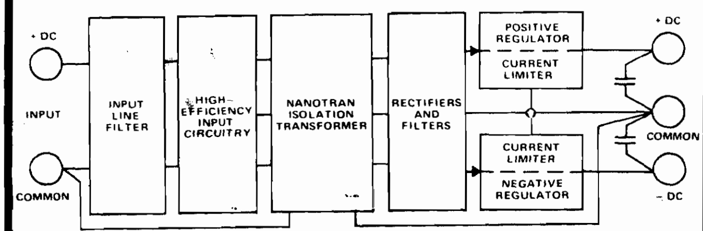
116000003

Power Supply DC/DC

Pin Configuration
Bottom View



Block Diagram

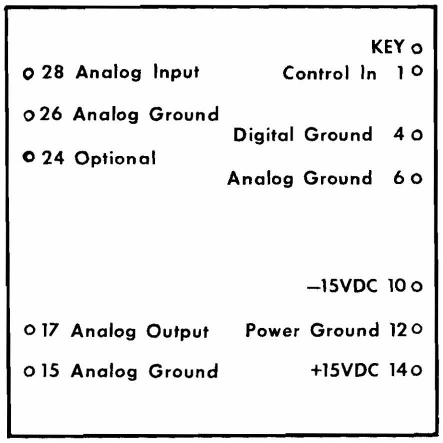


Pin Designations

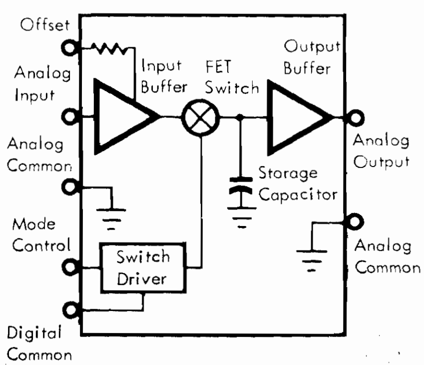
Pin No.	
1	+5VDC Input
2	Input Return
3	+15VDC Output
4	Common Grd
5	-15VDC Output

116000004

Pin Configuration
Bottom View



Block Diagram



Sample and Hold

Pin Designations

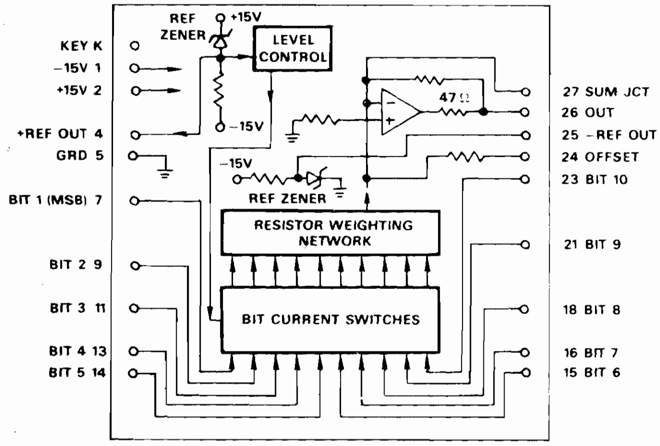
Pin No.	
K	Key
1	Control In
2	No pin
3	No pin
4	Digital Ground
5	No pin
6	Analog Ground
7	No pin
8	No pin
9	No pin
10	-15VDC
11	No pin
12	Power Ground
13	No pin
14	+15VDC
15	Analog Ground
16	No pin
17	Analog Output
18	No pin
19	No pin
20	No pin
21	No pin
22	No pin
23	No pin
24	Offset (Grd)
25	No pin
26	Analog Ground
27	No pin
28	Analog Input

The 116000004 circuit module is a fast sample-and-hold device with low droop rate and overall accuracy compatible with 12-bit A/D conversion systems operating to 1/2LSB accuracy. This module accepts ±10 volt data, a TTL/DTL and C/MOS compatible control signal, and requires ±15Vdc power.

116000006

D/A Converter

Pin Configuration & Block Diagram
Top View



Pin Designations

Pin No.	
1	-15V
2	+15V
3	No pin
4	+Ref Out
5	Grd
6	No pin
7	Bit 1 (MSB)
8	No pin
9	Bit 2
10	No pin
11	Bit 3
12	No pin
13	Bit 4
14	Bit 5
15	Bit 6
16	Bit 7
17	No pin
18	Bit 8
19	No pin
20	No pin
21	Bit 9
22	No pin
23	Bit 10
24	Offset
25	-Ref Out
26	Out
27	Sum JCT
28	No pin

The 116000006 circuit module is a 10-bit binary, unipolar digital-to-analog converter with a built-in I.C. output amplifier.

PART NUMBER	REV	DESCRIPTION
121-000001-	00	CRYSTAL 14.08 KC
121-000002-	00	CRYSTAL 16.00 KC
121-000003-	00	CRYSTAL 10 MC
121-000004-	00	CRYSTAL 20 MC
121-000005-	00	CRYSTAL 19.200 KC
121-000006-	00	CRYSTAL 8.8 KC
121-000007-	00	CRYSTAL 230.4 KC
121-000008-	00	CRYSTAL 153.6 KC
121-000009-	00	CRYSTAL 65.536 KC
121-000010-	00	CRYSTAL 307.2 KC
121-000011-	00	CRYSTAL 38.4 KC
121-000012-	00	CRYSTAL 76.8 KC
121-000013-	00	CRYSTAL 192.0 KC
121-000014-	00	CRYSTAL 13.33 MC
121-000015-	00	CRYSTAL 40 KC
121-000016-	00	CRYSTAL 204.8 KC
121-000017-	00	CRYSTAL 25.6 KC
121-000018-	00	CRYSTAL 10.752 KC
121-000019-	00	CRYSTAL 1228.800 KHZ VR6 E-5
121-000020-	00	CRYSTAL 11.5 MHC
121-000021-	00	CRYSTAL 100 KC
121-000023-	00	CRYSTAL 614.4 KC
121-000024-	00	CRYSTAL XTA2 1.54 MHZ
121-000025-	00	CRYSTAL 11.004 MHZ
121-000026-	00	CRYSTAL 50 MHZ
121-000027-	00	CRYSTAL 15.36 MHZ
121-000028-	00	CRYSTAL 160.000 KHZ
121-000029-	00	CRYSTAL 8.33 MHZ
121-000030-	00	CRYSTAL 6.912 MHZ
121-000031-	00	CRYSTAL CER RESNR 460KHZ +.2-.2%
121-000032-	00	CRYSTAL 3.685 MHZ 01030-006
121-000033-	00	CRYSTAL 9.38 MHZ +.01-.01 SERIES RES
121-000034-	00	CRYSTAL 20MHZ OSC K1114A
121-000035-	00	CRYSTAL OSC 13.33MHZ

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